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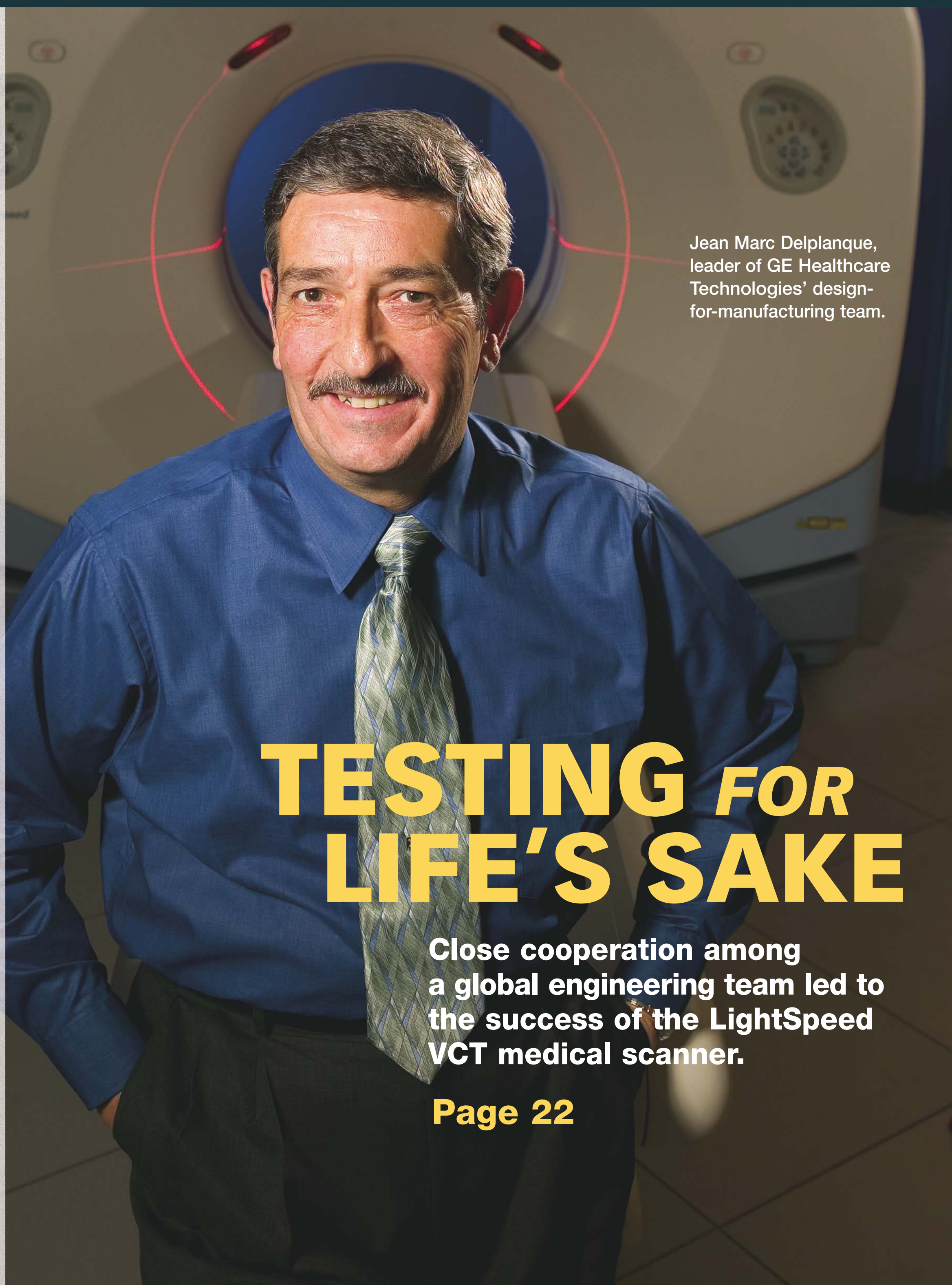

Jean Marc Delplanque, leader of GE Healthcare Technologies' design-for-manufacturing team.

TESTING FOR LIFE'S SAKE

Close cooperation among a global engineering team led to the success of the LightSpeed VCT medical scanner.

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COVER BY: TIM EVANS

Test & MEASUREMENT WORLD®

AUGUST 2005
VOL. 25 • NO. 7

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- Meeting the lead-free inspection challenge

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Test & Measurement World

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Reed Electronics Group

Open system, or competitor?

The Semiconductor Test Consortium chose Semicon West last month to tout its progress since its debut at Semicon West 2002. That progress has been significant, as the STC has pursued its goal of supporting the development of its OpenStar architecture, which defines hardware and software standards that compliant semiconductor test products must meet.

Specific goals range from the release of the original specification and Advantest's T2000 test system to the recent introductions of instruments such as Apria Technology's OpenStar-compliant arbitrary waveform generator and digitizer modules and a 6.5-Gbps Serdes test module from Advantest itself. As a measure of the platform's growing acceptance, the consortium announced in June that Toshiba is installing T2000 systems for wafer and package test. As for STC membership, the recent additions of OptimalTest and PX Instrument Technology have swelled the roster to 38 companies.

RICK NELSON, CHIEF EDITOR

STC chairman Bill Price, who represents member company Philips, told a Semicon West audience that vendors with open-architecture offerings will be well positioned to profit from what he sees as a shift in revenue away from ATE platforms and toward instruments, software, and services.

Customers have yet to insist on full OpenStar compliance.

But John E. Bearden, who became an independent test consultant after retiring from IBM, told the audience that based on surveys he has conducted, major users now see open-architecture approaches as "nice to have, but not must have." Their concerns, he said, center on instrument-module availability and price. He also mentioned concerns of the third parties who are considering building OpenStar instruments—these companies, he said, would be more likely to participate if they had a good way to estimate demand.

The ultimate test of OpenStar success would be an embrace of the standard by big-iron ATE vendors in addition to Advantest. But ATE makers are actively pursuing their own approaches, such as Teradyne's OpenFlex initiative, under which GuideTech has qualified its Femto 2000 continuous timing interval analyzer for the Teradyne Flex ATE platform. Credence Systems is pursuing its own open-architecture efforts with its Sapphire platform and has designed its Sapphire D-10 to work with off-the-shelf CompactPCI instruments.

It's worth noting that major semiconductor manufacturers have yet to insist that all future test-equipment purchases be OpenStar-compliant. Even STC chairman Price of Philips won't go that far.

Consequently, OpenStar systems are shaping up to be worthy competitors to the 93000s, Flexes, Fusions, and Sapphires out there, but the dream of an industry-wide single test platform remains just that. T&MW

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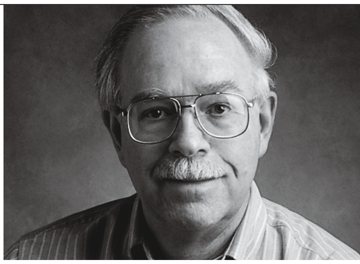


Remember your first "experiment"?

The test and measurement profession owes much to the scientific method of observing, devising a theory to explain the observation, experimenting to test the theory, and publishing the results—unless you're nine years old, in which case you proceed directly to the experimental phase just to see what the hell will happen.

As a recent amateur-radio newsgroup thread shows, the latter method inspired many careers in electronics. I won't embarrass anyone by using names, but the next time a would-be engineer sets fire to your garage, remember the following contributors who survived to become skilled technical professionals:

"I was four years old, and was playing 'motorboat'. Mine had two imaginary engines. Stuck a metal key into one outlet slot—revved it up. Now to fire up engine No. 2. . . bam! Blue lights flashing across the darkness of my clenched eyes. I don't recall the jolt, but boy, do I remember the 'blue lights'."

"I tried recharging a 9-V alkaline battery. I thought I was successful, but the battery made a loud bang three days later, inside a clock on the wall."

"Mine was a 150-V electrolytic capacitor at the age of 14 or so. Put it across a 275-V power supply that I had built on a round cake tin. The explosion was very loud and it took hours to clean up all the paper and electrolyte that had sprayed all over the shed walls, floor, and ceiling!"

"My earliest battery experiment was not as sophisticated: "D" cell with a nail driven into each end. Lamp cord twisted around nails and then plugged in. I can still recall the very loud resulting bang. My mother, who was out at the time, was very impressed by the strange smell hanging around when she returned home."

"I'm sitting at the kitchen table talking with my wife. Suddenly over her shoulder I see a major flash come from the hall that leads to the kid's rooms. There's my youngest (eight years old) standing with eyes wide open. On the ground next to him is a line cord [with] alligator clips. Attached to the alligator clips is the carcass of a 9-V battery. Surrounding the whole mess is a black powder coating the floor. Smoke hovers over the scene. As soon as I got out of the room, I couldn't help laughing to myself. That could easily have been me decades earlier. Maybe he's ready for some lessons in electricity." T&MW

DON'T TRY THESE AT HOME (UNLESS ACCOMPANIED BY A NINE YEAR OLD)

Are we in danger of losing our next generation of technologically savvy people to video games, cell phones, and instant messaging? It may take more than a few minor explosions or fulminating arcs to revive kids' interest in applied science and technology, but here are a few starters.

Entitled "Unwise Microwave Oven Experiments," this site describes Man's inhumanity to an innocent kitchen appliance:
www.amasci.com/weird/microexp.html

For a less-explosive experience, learn how an oatmeal box, a hunk of crystalline galena (lead ore), and a few more components can receive radio signals:
www.midnightscience.com
www.thebest.net/wuggy/build.htm

No visit to the stranger side of electronics would be complete without a Tesla coil or two—learn about a 122-footer at:
www.lod.org

Not exactly electronic in nature, but surely you can add flight instrumentation to your potatoes:
platinumchromatography.com/potato.htm

If the process of accelerating hapless vegetables to high speeds strikes you as routine, consider building an electromagnetic rail gun:
www.powerlabs.org/railgun.htm

. . . or crushing beverage cans and atomizing water via high voltage:
www.powerlabs.org/highvoltage.htm

You can shrink heads (and tails) by exposing coins to extreme electromagnetic forces: teslamania.delete.org/frames/shrinkergallery.html

If u cn rd this, u may be an extraterrestrial. How an organization devoted to greeting any ETs among us used a screened room, a spectrum analyzer, and an EMI receiver to explore one man's claims of having received an alien transceiver implant:
www.ieti.org/news/testing.htm

Omron Electronics achieves record growth, adds partners

Omron Electronics has announced record industrial-automation sales growth for its fiscal year ending March 31, 2005, resulting from a reorganization, product innovation, and focus on key markets, including machine-vision technologies tailored to applications areas ranging from food and beverages to semiconductors. A just-announced partner program that bundles Omron technologies with nine other automation companies' offerings are among ways the company plans to double its North American revenue within two years, according to Craig Bauer, president and COO of Omron Electronics, in comments during a two-day media event held at the company's Schaumburg, IL, headquarters June 29–30.

During the event, Omron partners demonstrated their offerings, and Omron introduced new products, including the $5840 F210-ETN Ethernet vision-sensor controller. The F210 has onboard storage for compressed inspection images, which can be streamed via Ethernet to a remote PC or laptop for analysis and long-term storage without interfering with ongoing production output. The controller features parallel processors for measurement and communication functions, enabling continued inspection without interruption while processing and sending data. Access from a remote location using Omron's Vision Composer Net software lets users start or stop sensing and set or change scan parameters without the need to directly access onboard controls. www.omron.com/oei.

Infrared tool measures wafers in one pass

To help the semiconductor industry measure 300-mm wafers, researchers at the National Institute of Standards and Technology (NIST) have developed an infrared instrument that measures differences in thickness across a 300-mm wafer. The researchers hope the tool will eventually allow them to establish a new calibration service for "master wafers" used in the industry to measure wafer thickness.

The Improved Infrared Interferometer (IR^3) uses intersecting waves of light to create interference patterns, which in turn can be used as a ruler to measure nanoscale dimensions. While most interferometers use red laser light, the IR^3 uses infrared laser light. The longer wavelengths of infrared light pass through a silicon wafer, allowing the IR^3 to illuminate both the top and bottom of a wafer and produce a detailed spatial map of differences in thickness in one pass. Changes in color within the spatial map represent changes in wafer thickness.

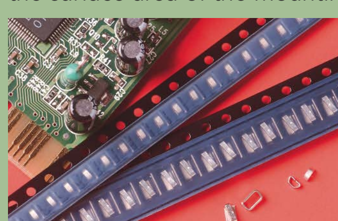
The NIST researchers make precision measurements of the wafer's index of refraction—the amount that light is "bent" as it passes through the silicon—as a critical step in correctly interpreting the interference patterns. Increased precision in the refractive index measurement will be necessary before absolute measurements of thickness rather than relative differences will be possible with the new instrument.

The NIST researchers were expecting to present their findings at the

RoHS-compliant SMT test points

EDITORS' CHOICE

Featuring a loop design to facilitate the connection of test probes to PCBs, the TP-107 series of low-profile, surface-mount printed-circuit board test points are fully compliant with the European Union directive "Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS). Their proprietary forming process, which consists of forming the flat wire design in a spiral wrap at the mounting base, effectively doubles the surface area of the mounting base to enable a PCB solder connection that can withstand 18 lbs of force. A loop design provides a secure connection for miniature spring-loaded clips, probes, and hooks.



The test points offer a 0.090-in. (2.29 mm) profile. Specifications include a 2-A current rating and a –55°C to +125°C operating temperature. The parts feature a matte tin over nickel finish and are manufactured using a 0.015x0.040-in. phosphor bronze, spring-tempered, flat-wire alloy.

Designed for automatic insertion by industry-standard pick-and-place equipment and reflow soldering, the test points are supplied on 12-mm-wide, 4-mm-pitch, conductive polycarbonate tape. The units may be ordered on either 7-in., 1000-piece reels or 13-in., 5000-piece reels.

Price: $0.078 each in quantities of 1000. *Components Corp.*, COMPONENTSCORP.COM/DETAILS/TP107.HTML.

American Society for Precision Engineering (ASPE) Summer Topical Meeting on Precision Interferometric Metrology in late July. www.nist.gov.

Agilent, Asylum to collaborate on nanotechnology measurements

Agilent Technologies recently announced that it has made an equity investment in Asylum Research (Santa Barbara, CA) and that its Nanotechnology Measurements Division (NMD) will collaborate with Asylum on technologies for use in nanotechnology measurements. Asylum Research is a manufacturer of atomic force microscopes (AFMs), which are used to measure the shape and properties of materials at the nanometer scale.

The agreement will enable Agilent to develop new features for AFMs as well as gain more knowledge about AFM customer needs. "The joint development agreement underscores our commitment to new technologies and markets," said Bob Burns, VP and GM of Agilent's NMD. "The AFM market is a significant portion of the $1 billion market for nanotechnology measurement tools, with the segment growing at close to 20 percent a year." www.agilent.com.

CALENDAR

EOS/ESD Symposium, September 11–16, Anaheim, CA. Sponsored by ESD Association. *www.esda.org.*

Autotestcon, September 26–29, Orlando, FL. Sponsored by IEEE. *www.autotestcon.com.*

International Robots & Vision Show, September 27–29, Rosemont, IL. Sponsored by Automated Imaging Association and Robotic Industries Association. *www.machinevisiononline.org.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

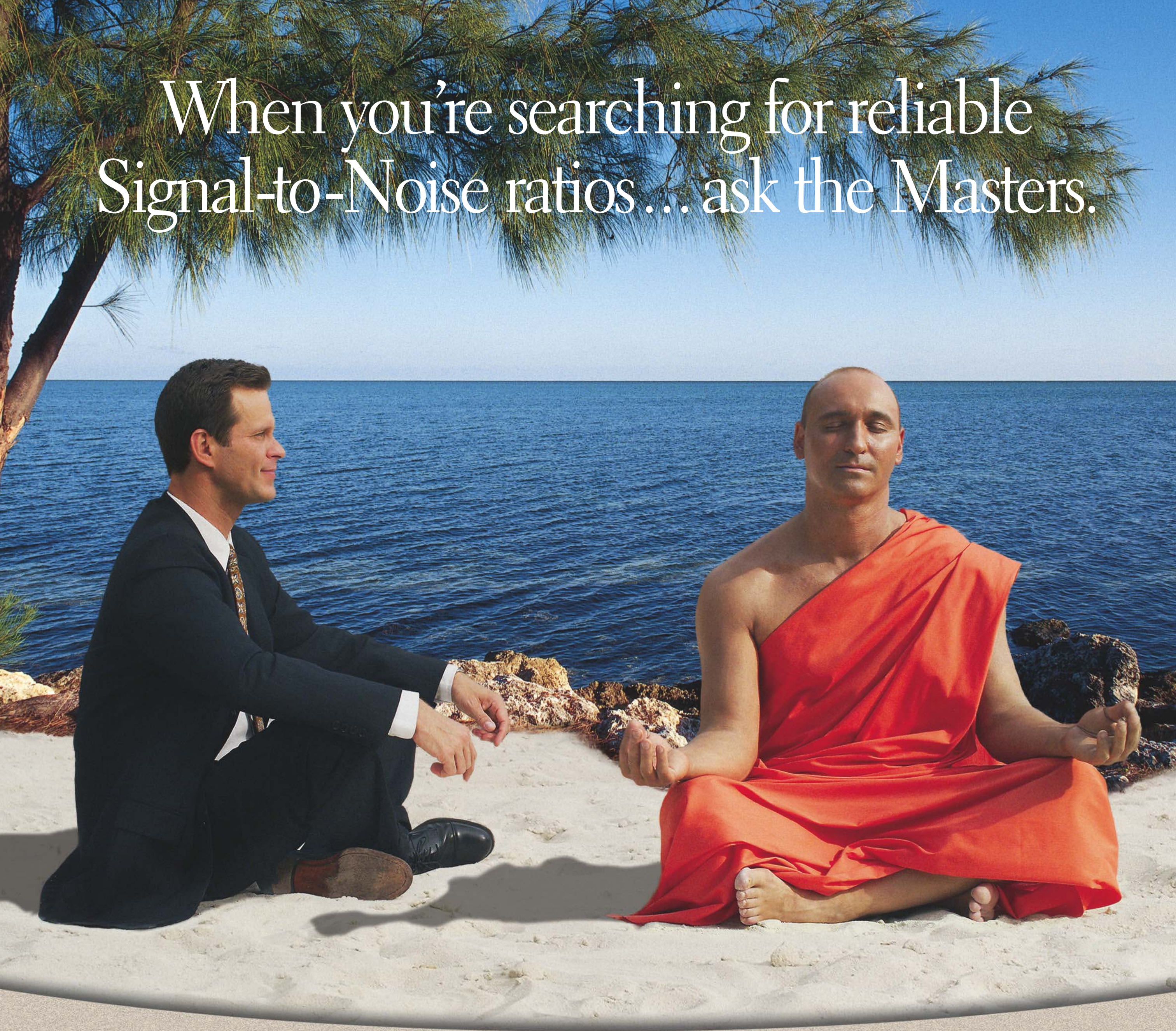
EDITORS' CHOICE

Fusion EX quadruples CX capacity

LTX's 80-slot Fusion EX test system offers four times as many instrument channels as the vendor's Fusion CX. The Fusion EX's 80 universal instrument slots accommodate existing Fusion platform instruments, which offer a limited number of instrument channels per card to provide fine instrument-channel granularity to allow incremental enhancements in capabilities. The EX provides full functional test capabilities and features the built-in support necessary for structural test, including digital performance up to 200 MHz (including embedded-memory test and time-measurement-per-pin capabilities). A Serdes test option operates to 12 Gbps. The Fusion EX also offers DFT support through independent scan-per-pin capability, and it provides a seamless interface to third-party BIST tools with fully integrated diagnostic support.

In addition, Fusion EX uses the same mixed-signal instrument set as the Fusion CX and Fusion DX configurations, including multiple synthesizers and digitizers and a full suite of DC and power test options. The EX also provides program compatibility through LTX's enVision device-oriented programming environment, which provides debug tools, encapsulation of test objects to support reuse of test intellectual property, and transparent multisite capabilities.

Price for typical configurations: $500,000 to $800,000. *LTX,* WWW.LTX.COM.



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Software complements instruments at microwave show

> > > The International Microwave Symposium, June 12–17, Long Beach, CA, www.ims2005.org.

Anritsu (www.us.anritsu.com) presented Version 2.0 of the company's MS2781A Signature signal analyzer, which operates up to 30 times faster than Version 1, according to the company. It also debuted its new UMTS Master, enhanced-data-rate (EDR) test software for its MT8850A and MT8852A Bluetooth test sets, and three CDMA2000 1xEV-DO measurement options (RF, demodulation, and over-the-air) for its Cell Master MT8212B handheld analyzer. **Boonton Electronics** (www.boonton.com) introduced its Model 4500 peak power analyzer, which can capture, display, and analyze RF power information in both the time and statistical domains.

Agilent Technologies (www.agilent.com) demonstrated its N6031A arbitrary waveform generator, which simultaneously delivers 1.25 Gsamples/s and 10 bits of vertical resolution. The company also introduced a 14-bit, 40-MHz-bandwidth digitizer for its PSA Series spectrum analyzers, announced extended frequency ranges on its 80-MHz-bandwidth digitizers, and introduced a 64-bit version of its Momentum 3-D-planar electromagnetic modeling software.

The ZVT8 eight-port vector network analyzer supports multiport and balanced-device measurements from 300 kHz to 8 GHz.

Courtesy of Rohde & Schwarz.

Aeroflex (www.aeroflex.com) announced extensions to its phase-noise offerings—including the low-cost ($27,500) Model PN8000 tester and a new downconverter. The company also announced enhancements to its synthesizer lineup, reporting that the enhanced 2500 series frequency synthesizers are faster, cleaner, and smaller than their predecessor, the FS5000. **Rohde & Schwarz** (www.rohde-schwarz.com) introduced its ZVT8 eight-port vector network analyzer, its FSL 15.5-lb 6-GHz portable spectrum analyzer, and its 6-GHz SMJ100A vector signal generator. T&MW

Debug group debuts at DAC

> > > Design Automation Conference, June 11–18, Anaheim, CA, www.dac.com.

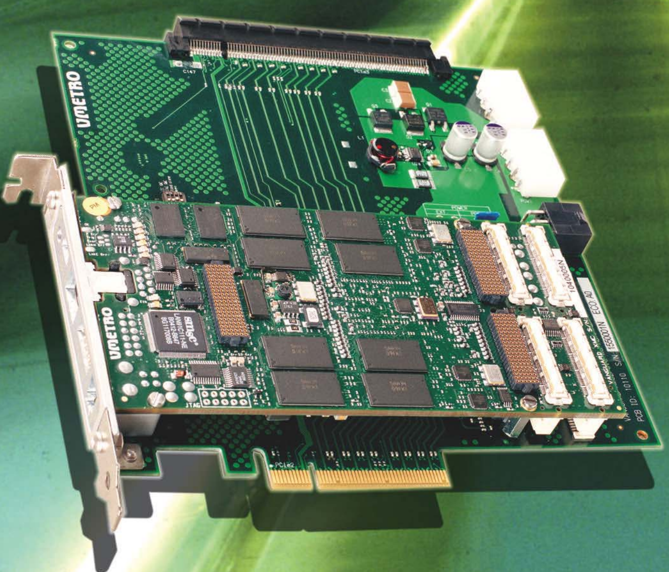
During this year's DAC, representatives of the design, manufacturing-test, and silicon-debug supply chain announced the formation of the **Design for Debug (DFD) Consortium** (www.designfordebug.org). The goal of the consortium is to address tool-interoperability and methodology issues. Charter members include Corelis, DAFCA, First Silicon Solutions (FS2), Intellitech, JTAG Technologies, Novas Software, and consultant Fidel Muradali.

Magma Design Automation (www.magma-da.com) announced limited availability of its new Blast Yield design-for-manufacturability (DFM) and design-for-yield (DFY) tool for IC designs at 90 nm and below. **Cadence Design Systems** (www.cadence.com) outlined its strategy for what it calls enterprise verification process automation (VPA), which addresses the link between design and verification and offers users an optimal blend of e, SystemVerilog, and SystemC languages. The strategy mirrors market-tested approaches established by leading enterprise software companies such as SAP and Oracle.

Genesys Testware (www.genesystest.com) highlighted its new ArraytestMaker tool for embedded test and repair of memory. **Tharas Systems** (www.tharas.com) demonstrated its new Hammer S-Class and M-Class verification appliances, which employ a multicore custom processor designed by the company. It also highlighted its new Virtual Connect, which it describes as an RTL-accurate emulation capability that works with the Hammer systems to perform hardware/software coverification for embedded systems.

Atrenta (www.atrenta.com) introduced its 1Team Embedded C and C++ analysis environment for embedded software. **Carbon Design Systems** (www.carbondesignsystems.com) introduced its VSP (for virtual system prototyping), which enables users to assemble a system prototype and functionally validate it at the desktop. T&MW

Get on the Vanguard Express



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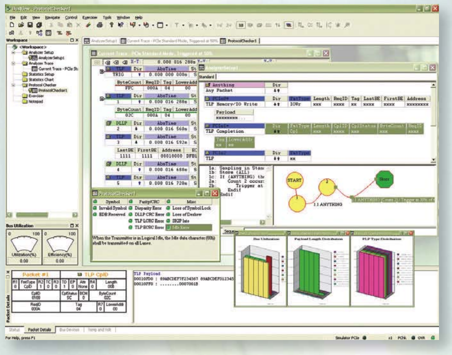

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EMC awareness has risen

Over the last 10 years, EMC awareness among electrical engineers has risen. The EU's EMC Directive, which forces manufacturers to comply with numerous standards, has driven engineers to design for EMC.

"Engineers are now comfortable with the EMC Directive," said Roland Gubisch, engineering manager for EMC and telecom at Intertek ETL Semko (Boxborough, MA). As a result, he sees few products failing EMC compliance tests.

Designers now accept EMC as part of their job. Ken Wyatt, senior EMC engineer at Agilent Technologies (Colorado Springs, CO), makes it clear to his company's designers that it's their job to design for compliance, not his. "I assist designers by providing training, running tests, and analyzing their designs," noted Wyatt. "At first, we brought in well-known consultants Henry Ott, Howard Johnson, and Doug Smith to train our engineers in EMC theory, PCB design, and signal integrity." Wyatt now conducts in-house seminars, both in person and online.

IBM has taken a similar approach. "We recognized a need to design for EMC, so we hired Dr. Bruce Archambault to train our engineers," said Len Powell, program director for design, support, test, and validation at IBM's Raleigh, NC, facility. "We also developed tools to model EMC in our designs. The modeling tools solve Maxwell's Equations and provide 'what if' scenarios." Archambault conducts classes in EMC design and meets with engineers at least once a year to keep them current on the latest design techniques.

Don Sweeney, president of test lab D.L.S. Electronic Systems (Wheeling, IL) also sees an overall rise in EMC awareness, but with two qualifications. Although he rarely sees engineers who don't know that designing for compliance is a requirement, Sweeney has noted that some engineers don't know the repercussions of not complying with EMC standards. For example, a lack of compliance means that you can't sell your product in Europe. He also finds that engineers at small companies are less EMC aware than those at large companies. "Large companies have the resources to train their engineers, but small companies don't," he said.

Engineers regularly attend EMC training sessions given by consultants and test labs. Courtesy of D.L.S. Electronic Systems.

An engineer's enthusiasm for learning about EMC is a function of his or her age. "Young engineers are eager to learn and to use our simulation tools," said Archambault. "Older engineers are more set in their ways and are reluctant to change."

Wyatt added, "Most of the reluctant engineers have retired, leaving us with a younger, more receptive group."

Engineers are now particularly good at designing for EMC emissions, but some still need help with immunity. EMC consultant Doug Smith said "I often have to help engineers with setting up immunity tests. There is little correlation between passing that test and having a product work in the field." T&MW

Program measurements with .NET

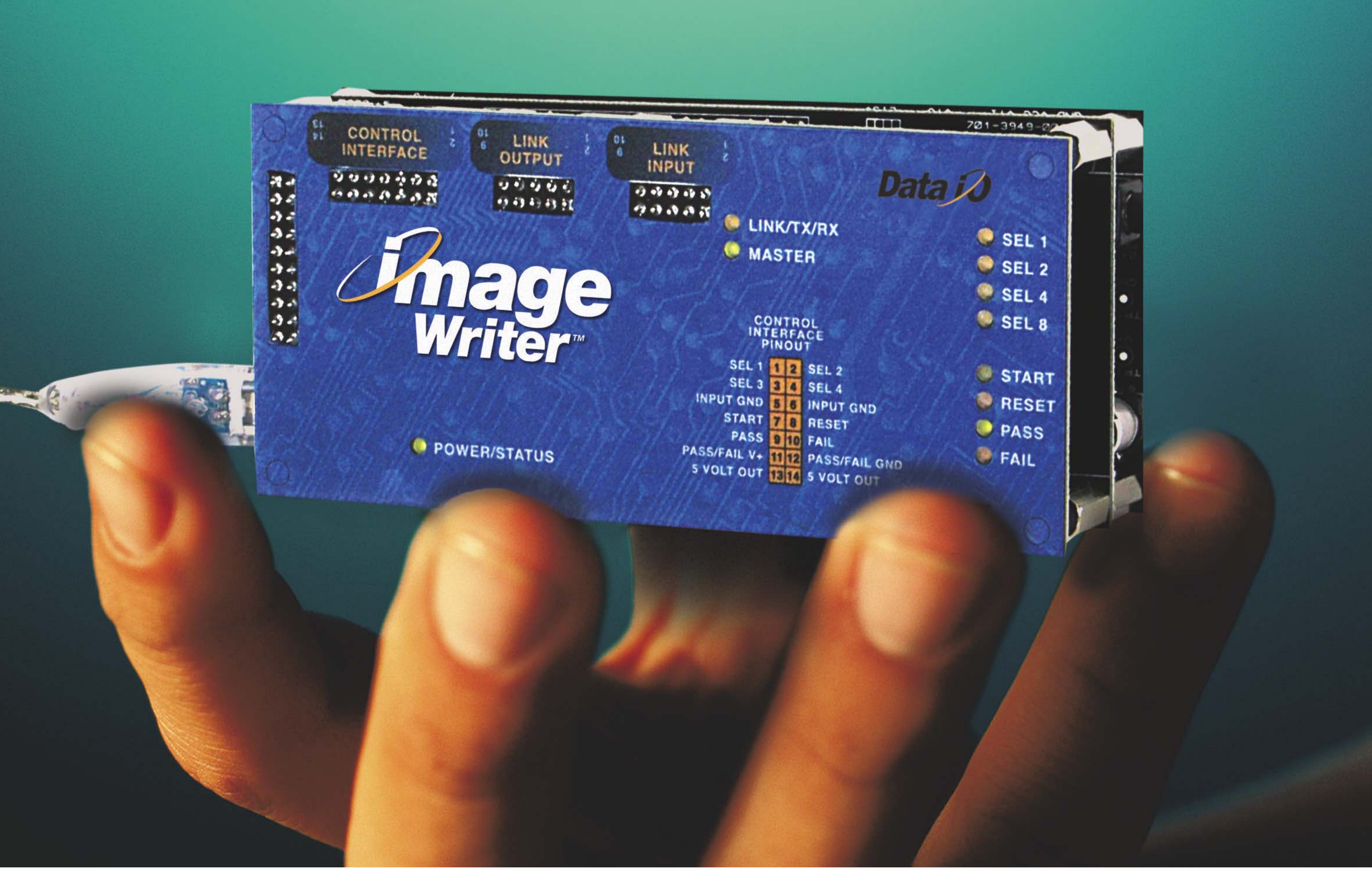
With the new DTx-EZ tool, you now can program Data Translation's data-acquisition hardware through Microsoft's .NET framework. The company has added .NET-compatible "wrappers" around its drivers. DTx-EZ is available with the company's data-acquisition hardware and as a free download. www.datatranslation.com.

Online videos cover product safety

With online instructional videos, you can learn how to properly connect test leads to the Hypot III line of hipot testers and Hyamp III ground-bond testers from Associated Research. The seven videos demonstrate connection to a DUT through test leads and through an adapter box for line-powered devices. www.asresearch.com/video.

Free power analyzer upgrade

Fluke has a firmware upgrade for its 430 series of power analyzers. Version 1.10 speeds menu navigation through new shortcuts, and it also improves the warning message system. You can toggle between phase-to-neutral and phase-to-phase readings. www.fluke.com/430upgrade.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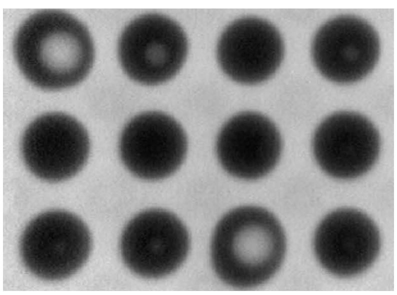
Moving beyond boundary scan and inspection

The most evident twin changes in the electronics industry in the past 20 years have been the increase of circuit functionality and the ever-declining access to board nodes to ensure that a circuit works.

Test engineers point to design-for-testability as one solution, but design engineers have never met that concept with enthusiasm. The same can be said of built-in self-test, which rarely covers more than about a third of possible failures. At one point, we thought we



This x-ray "slice" of the balls from a ball-grid array clearly shows solder voids. Courtesy of Agilent Technologies.

had the ultimate solution in boundary scan, but that, too, has been called into question—manufacturers are facing the limitations of boundary scan to verify a board's function as well as the likelihood that boundary scan makes boards more susceptible to security breaches.

So what do we do? How do we ensure proper circuit operation? Inspection has addressed some of the issues, like voids in ball-grid arrays, but it can find only a subset of possible faults. Hot mockup is time-consuming and extremely labor-intensive, and its results tend to be more qualitative than quantitative; also, mockup systems degrade as they age (called "hot mockup system wearout") until you can't tell if a failure comes from the system or the board under test. How do you schedule calibration/maintenance/replacement for hundreds of systems? On system failure? On a rotating basis? All at once?

Both OEMs and contract manufacturers have to get away from the notion that a single test strategy can address every situation. Contract manufacturers who truly want to be ready to accept any task that walks in the door must remain flexible enough to devise unique strategies specifically optimized for each situation rather than rely on a menu of predetermined choices. Those who specialize in certain kinds of boards will find the path somewhat less complicated—and less crowded.

Some new(ish) ideas are emerging. Some board-test manufacturers are turning to a variation of in-circuit emulation to address some of the problems. Today's device designers have to incorporate test routines in their silicon because it is the only way to determine if the device works. Ireland-based International Test Technologies has adapted emulation techniques to microprocessor-based boards by taking advantage of those device-level test routines, knitting them together the way in-circuit test programs were assembled years ago. Other companies are adopting similar approaches. Although not appropriate for every board category, on the subset of boards for which they work, these techniques are quite successful.

Mostly we need to take the action that experts recommend for all innovation—we must think outside the box. Because as the box grows ever smaller, much less of what we face every day will fit inside it. T&MW

Flying prober offers positioning resolution of 1.25 mm

The Takaya APT-9411 flying prober from Itochu Europe improves both speed and accuracy over its predecessors. The tester provides x and y positioning resolution of 1.25 mm for testing ever-smaller components on densely populated boards. It offers four moving probes, plus two IC opens on the top side. A camera comes standard to provide visual alignment and inspection. A flying height of 40 mm accommodates a wide variety of board types. www.itochu-takaya.co.uk.

Ronetix announces JTAG emulator

Offering a high-speed, low-cost JTAG emulator for ARM7 and ARM9-based microcontrollers, the Powerful Embedded Ethernet Interface (PEEDI) from Ronetix supports native GNU gdb (remote target via Ethernet). It provides a download speed of more than 400 kbytes/s and a 5-kHz to 33-MHz JTAG clock using 25-cm standard cable. Its telnet interface provides simple debugging and target flash programming. The built-in flash programmer supports more than 750 flash devices and can be used as a stand-alone unit. www.ronetix.at.

Study makes the case for quality

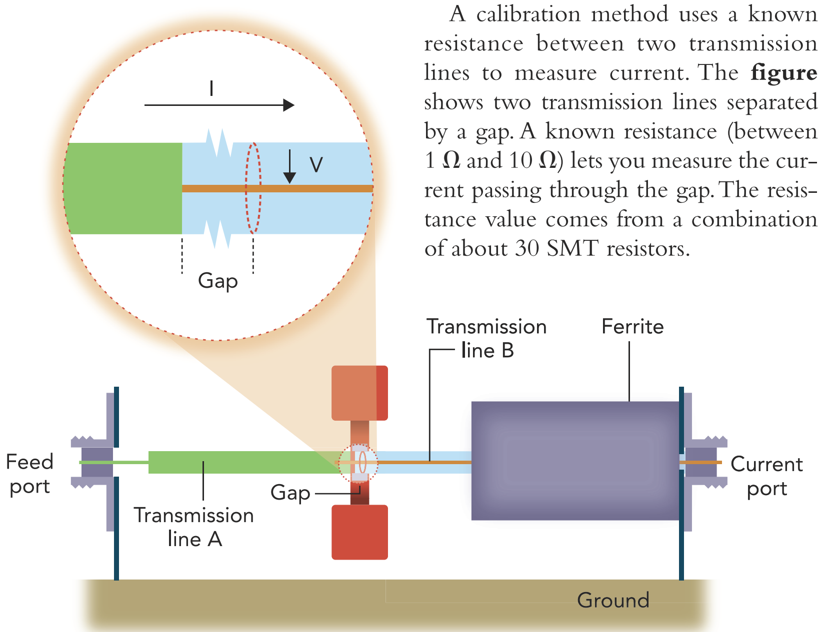
The American Society for Quality has released a case study called *The Economic Case for Quality* to demonstrate the impact of quality on a company's bottom line. The study came in response to requests from members who experienced difficulty in conveying the importance of quality as a business-management tool to upper-level executives. www.asq.org.

EMC

Calibrate current clamps

Current clamps let you perform emissions and immunity measurements in signal and power cables. Unfortunately, clamps absorb some energy from the circuit under test in order to make a measurement. Thus, they produce measurement errors. By applying a known current to a test fixture, though, you can calibrate your equipment and characterize the current clamp. You can also analyze the effect of placing the clamp on the cable.

A calibration method uses a known resistance between two transmission lines to measure current. The **figure** shows two transmission lines separated by a gap. A known resistance (between 1 Ω and 10 Ω) lets you measure the current passing through the gap. The resistance value comes from a combination of about 30 SMT resistors.



A series resistor across a gap between transmission lines provides a known resistance from which you can measure current and calibrate a current clamp. Courtesy of IEEE.

A feed port connects a network analyzer to a metallic rod, which provides a low-impedance path to the gap resistors. The resistors then connect to a coax cable, which carries the current to a 50-Ω termination. The network analyzer measures the voltage at the fixture's exit port. Using S-parameter analysis, you can calculate the current that passes through the gap resistors.

By placing a current clamp over the gap resistors, you can measure the clamp's output voltage. Current-clamp manufacturers provide the clamp's transfer impedance, so you can calculate the current measured by the current clamp. Then, you can compare it to the current in the gap resistors, measured by the network analyzer, and calibrate the current clamp.

To learn about the theory, construction details, and test results of this method, download "A New Test Setup and Method for the Calibration of Current Clamps," by David Pommerenke of the University of Missouri-Rolla, Ramachandran Chundru of Texas Instruments, and Sunitha Chandra of Nvidia, from web.umr.edu/~davidjp/publications.html.

Martin Rowe, Senior Technical Editor

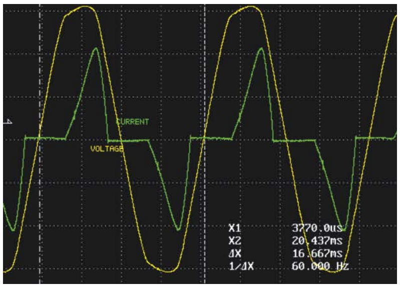
ARCHIVED WEBCAST

Power measurement and analysis

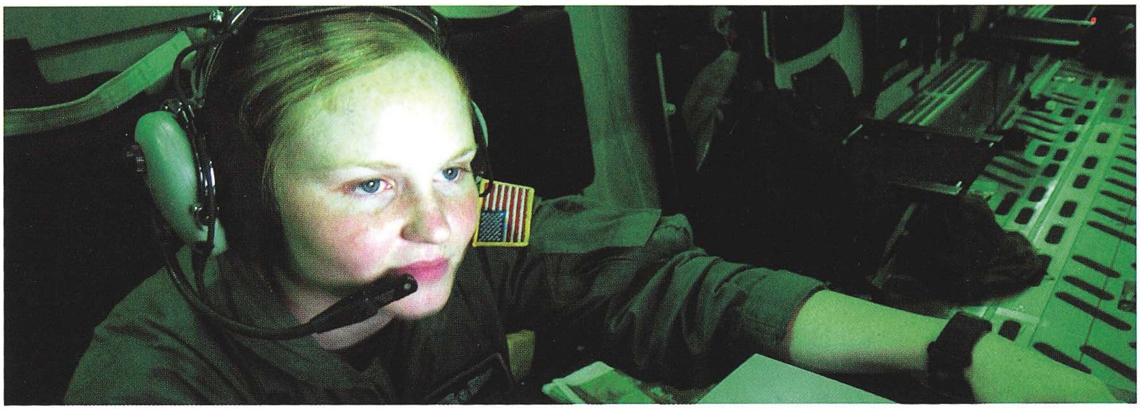
Whether you are dealing with a three-phase high-power industrial-distribution system or an Energy Star-compliant computer in standby mode, you're likely to have to make power measurements. Instruments that can make such measurements range from current sensors and wattmeters to precision power analyzers as well as digital oscilloscopes equipped with power-analysis capabilities.

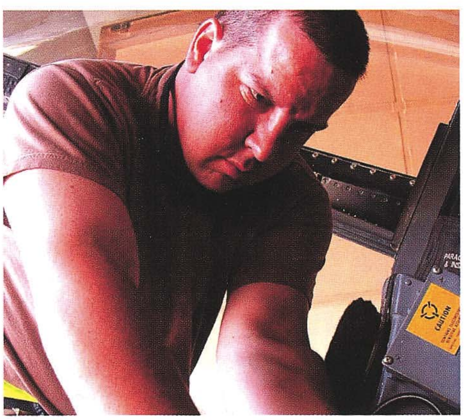
In the Webcast, "Power Measurement and Analysis," produced by *Test & Measurement World*, sponsored by Yokogawa's Test and Measurement Division, and originally broadcast May 24, Bill Gatheridge, Yokogawa's product manager for power-measuring instruments, describes how to apply those instruments to make single-phase and three-phase measurements in the presence of inductive and capacitive loads powered by sinusoidal or pulse-width-modulated sources.

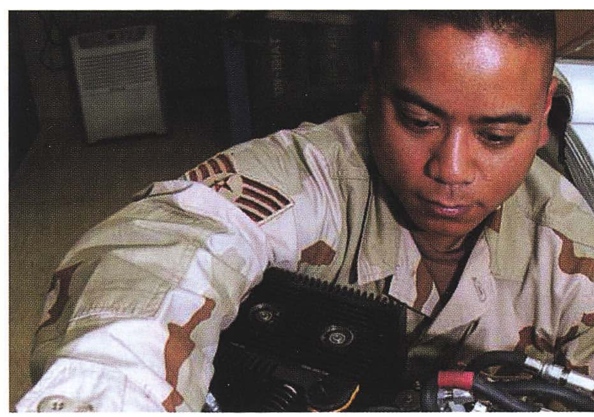
Gatheridge begins with the basics, covering Ohm's law as it relates to AC power measurements. He reviews the Blondel transformation, which states that to measure power, you need one



You can't derive displacement power factor from a scope display when dealing with nonsinusoidal signals like this green current waveform; therefore, you'll need to calculate true power factor by dividing measured power in watts by measured volt-amperes. Courtesy of Yokogawa.







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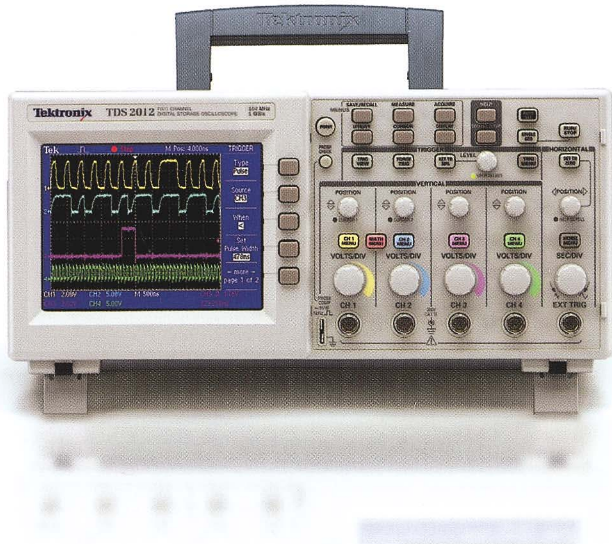

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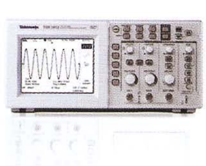

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Specific applications covered include analysis of low-power systems, switching power supplies, and inverters and pulse-width-modulated drives. Gatheridge also covers power factor, which comes into play with inductive loads (such as AC motors), where current lags voltage, as well as with capacitive loads (such as fluorescent lighting), where current leads voltage. He describes the difference between displacement power factor (the cosine of the phase shift between pure voltage and current sine waves) and true power factor (power in watts divided by total volt-amperes). He concludes by describing a three-wattmeter method for measuring power factor in three-phase systems.

An archive of the Webcast is available at www.tmworld.com/webcasts.

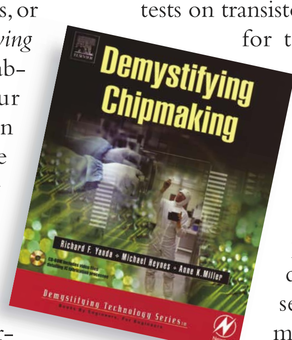
Rick Nelson, Chief Editor

BOOK REVIEW

A bird's eye view of IC fabrication

Demystifying Chipmaking, by Richard F. Yanda, Michael Heynes, and Anne K. Miller, Newnes (www.newnespress.com), 2005. 256 pages. $49.95.

Semiconductors are pervasive, but detailed knowledge about how they are fabricated is not—except among the manufacturing and process engineers who produce them. If you're designing and testing boards, subsystems, or complete products, *Demystifying Chipmaking* won't have you fabricating Pentiums in your garage, but it will provide an interesting overview of the IC fabrication process while familiarizing you with the terminology.



Topics range from contamination control to the dual-damascene metal-interconnect process, which has come a long way from the Middle Ages technique for which it's named. The book introduces timely topics, covering low-*k* dielectrics and why they are important (to improve chip speeds by minimizing parasitic capacitance), and it describes the pellicles that prevent reticle contamination from causing chip defects (by keeping contaminating particles sufficiently far from the reticle that they are out of focus and consequently not printed on a target wafer's surface).

Test-related topics include a brief description on the use of statistical process control to employ test and inspection results to maintain yields. A chapter on test and assembly describes parametric tests on transistors embedded in a wafer for that purpose as well as functional tests at wafer probe and final package test, but it omits any mention of scan tests or other design-for-test (DFT) approaches. In a chapter on design, the book cites several groups for chipmaking credit—layout, logic, applications, architectural, and technology-transfer engineers—but it neglects to mention DFT engineers.

The book comes with a CD-ROM that provides video of various chipmaking stages. For your colleagues who aren't engineers, there's an appendix that provides the basics of the chemistry and physics behind semiconductor fabrication and behavior. (Disclosure: The book's publisher is owned by *Test & Measurement World*'s parent company.)

Rick Nelson, Chief Editor

RF TEST

Four-port calibrated structures

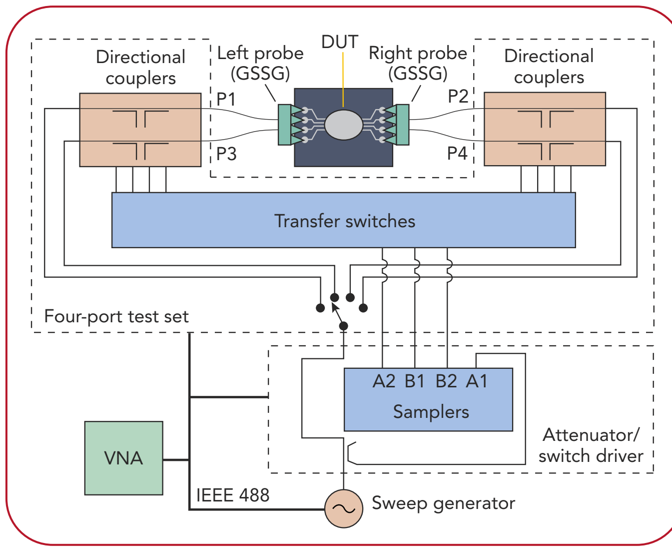
DEVICE UNDER TEST
Microwave amplifiers, filters, transmitters, receivers, and radar chip sets that operate at frequencies to 40 GHz. These balanced differential devices are made on silicon or gallium arsenide substrates and are on wafer during tests.

THE CHALLENGE
Develop a test method and the equipment to calculate S-parameters for four-port differential microwave devices based on multimode techniques. Calibrate a test station that consists of a vector network analyzer at frequencies to 40 GHz. Overcome problems found in commercial calibration standards.

THE TOOLS
- Agilent Technologies: vector network analyzer, attenuator/switch driver. www.tm.agilent.com.
- Cascade Microtech: automatic wafer prober and ground-signal-signal-ground (GSSG) RF wafer probes. www.cascademicrotech.com.
- Electroglas: automatic wafer prober. www.electroglas.com.
- M/A-Com: custom RF calibration structures. www.macom.com.
- The Mathworks: technical computing software. www.mathworks.com.
- Pico Probe: GSSG RF wafer probes. www.picoprobe.com.

PROJECT DESCRIPTION
Before engineers at M/A-Com (Lowell, MA) can characterize balanced, 24-GHz ICs with a vector network analyzer (VNA), they need to calibrate their test system. To compensate for errors introduced by cables, switches, connectors, and wafer probes, the engineers measure the responses of calibration standards and compensate for errors in software. After making the calibration using custom calibration standards and compensating for measurement errors, engineers repeat the measurements on the calibration standards to verify accuracy in the process.

"When we used commercially available calibration standards at frequencies above 10 GHz, we found that the magnitude of S_{21} would be greater than unity when we measured the calibration standards again," said principal engineer Alan Jenkins. "That's impossible, because the calibration standards are passive structures." To solve the problem, M/A-Com developed its own on-wafer calibration standards.



Switches let a modified two-port VNA make four-port measurements.

The standards are a uniform set of microwave transmission lines. One is a planar "through" standard with effectively no delay. Two delay standards introduce known, fixed propagation delays to signals passing through them. A fourth, "reflect" standard is a specific open circuit between the structure's test pads. All structures use two signal traces surrounded by two ground traces, thus making four ports. This configuration lets engineers perform a four-port calibration with results consistent with two-port calibrations for balanced circuits. With four-port measurements, the common- and differential-mode S-parameters are available. (The online version of this story contains diagrams of the standards, www.tmworld.com/archives.)

To make the VNA into a four-port instrument, M/A-Com engineers added an attenuator/switch driver. They drilled through the case and connected coax cables close to the instrument's input circuits. The coax cables connect to the attenuator/switch driver, which then connects to a patch panel. The VNA, attenuator/switch driver, and patch panel reside in an instrument rack located next to a wafer-probing station.

Jenkins, along with principal engineers Tekamul Buber, Noyan Kinayman, and others, developed a "multimode through-reflect-line" calibration theory, dubbed MTRL. After making measurements on the calibration standards, they use custom software to calculate eigenvalues that they apply to DUT measurements. The software uses the eigenvalues to correct the DUT measurements to produce the final results.

LESSONS LEARNED
"We learned more about calibration methods than we thought we would," said Jenkins. "Finding a gain above 10 GHz for a through line was an eye opener." By using their own calibration standards, M/A-Com engineers were able to prove that the errors were caused by the commercially available calibration standard, not by the compensation algorithms they had developed. "The technique lets us separate common-mode gain from differential gain," added Kinayman.

Martin Rowe, Senior Technical Editor

TESTING *FOR*

CLOSE COOPERATION AMONG A GLOBAL ENGINEERING TEAM LED TO THE SUCCESS OF THE LIGHTSPEED VCT MEDICAL SCANNER.

LAWRENCE D. MALONEY, CONTRIBUTING EDITOR

WAUKESHA, WI—For doctors dealing with medical emergencies, the speed and accuracy of diagnostic equipment play crucial roles in a patient's chances for survival. Speed is measured in the precious seconds required to obtain high-resolution images of damaged hearts, shattered bones, or ruptured vessels, while accuracy hinges on the ability of sophisticated x-ray detectors to prevent artifacts that could lead to a misdiagnosis.

Now, thanks to the work of engineers at the sprawling GE Healthcare Technologies complex just west of Milwaukee, more doctors can tap what is being described as "the quintessential emergency room tool." Introduced in the first quarter of this year, the LightSpeed VCT (volume computed tomography) generates 3-D-quality images that are setting new standards for CT scanners.

In a single 0.35-s rotation, the VCT simultaneously acquires 64 slices of data, each 0.625 mm wide, for a total anatomical coverage of 40 mm. That's four times the coverage of GE's current LightSpeed Pro 16 scanner. As a result, the scanner can capture images of most organs in 1 s, the heart and coronary arteries in just 5 s, and the whole body in 10 s.

The speed and quality of these images have so impressed the medical community that many physicians see the LightSpeed VCT as an alternative to costly invasive procedures, such as angiograms (see "Patients: The real winners in 'slice wars,'" in the online version of this article at www.tmworld.com/archives). By early May, GE Healthcare had already installed 30 of the scanners, priced at about $2 million each, with another 250 orders booked.

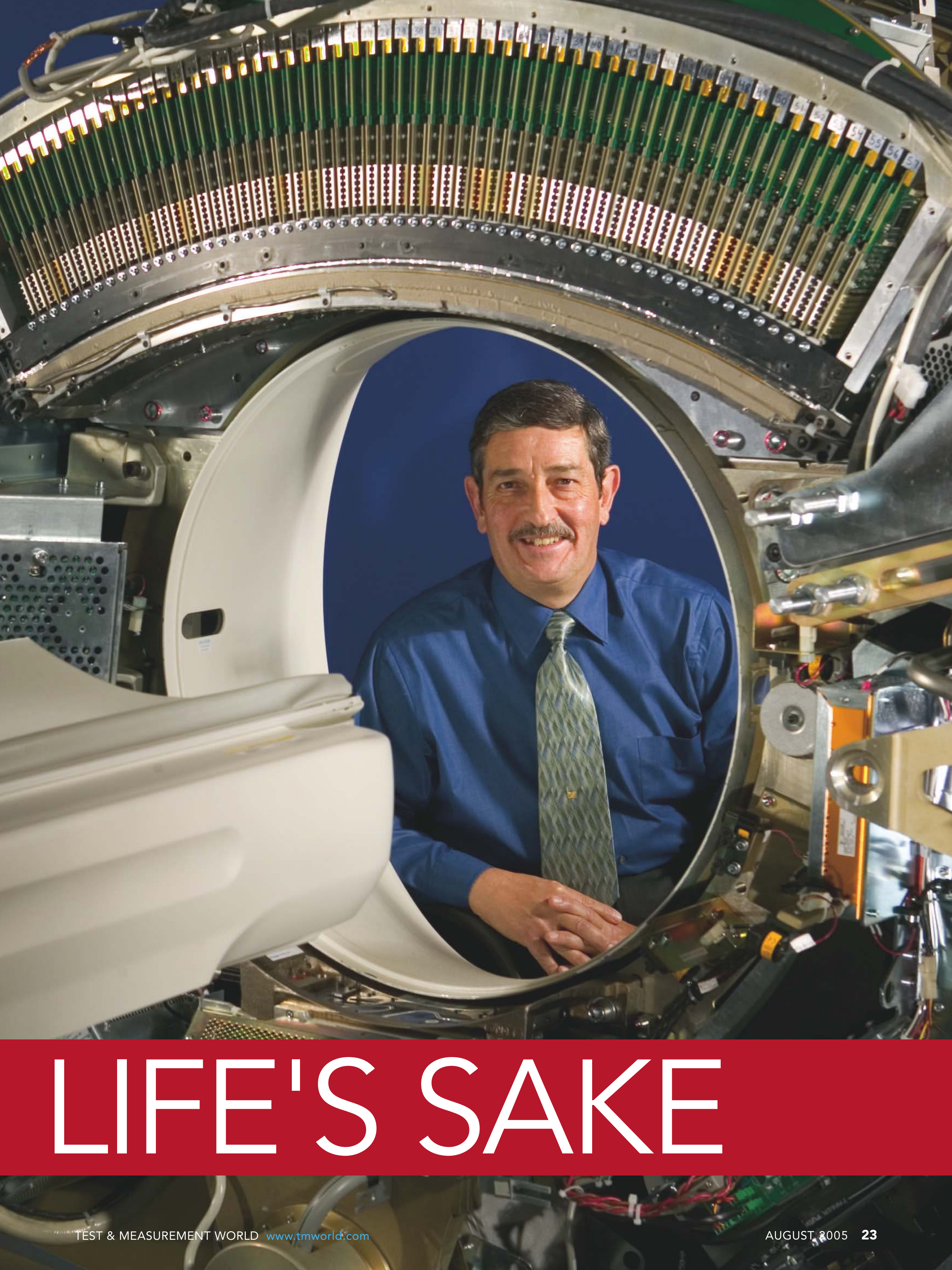
"This is the biggest order backlog for a CT scanner that we've ever had," said Scott Schubert, GE Healthcare's global product manager for CT. He added that the scanner's enhanced capabilities will lead to further expansion of CT procedures, already growing at a rate of more than 10% annually. Worldwide, patients undergo 100 million CT exams each year—with half of that number performed in the US alone.

Detector technology

From a testing standpoint, some of the biggest challenges presented by the LightSpeed VCT centered on its new detector system, called the V-Res. Along with the x-ray source, situated directly opposite it, the detector revolves around the patient within a donut-shaped gantry.

TIM EVANS

Jean Marc Delplanque, leader of the design-for-manufacturing team, noted that the manufacturing tests required for the VCT's detector boards were based on the needs of the product, not on the engineering team's organizational structure.



LIFE'S SAKE

The V-Res features a proprietary HighLight composite ceramic material in the scintillator, the component that converts the incoming x-ray to visible light. An adjacent photodiode detects the light, converts it to an electrical signal, and transmits it to the data-acquisition system. On the VCT, GE pioneered a backlit diode, which routes the electrical signal from the rear of the diode. This permits a denser, more compact diode array and makes it possible to add more detector elements in future designs.

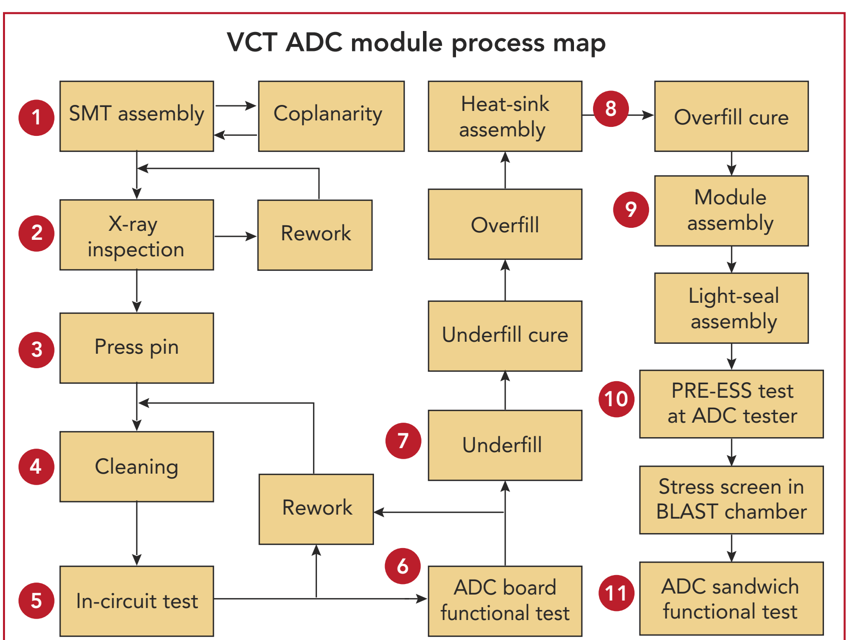
Engineers at GE's Schenectady, NY, R&D center also developed a new analog-to-digital converter (ADC) chip—the Volara—that was fabricated by Idaho-based AMI. Eight of these chips reside on a detector board that includes a heat sink and is about 20% smaller than that used in the previous-generation Pro 16, which has only two ADCs.

Previous detector designs also featured longer flexible circuits for interconnects, which plugged into card-rack backplanes. "Now, we are packaging the electronics in much tighter proximity to the photodiode and optoelectronics to minimize the capacitance and physical distance—and that translates into much lower electronic noise and higher signal isolation," explained Jeff Kautzer, manager of CT detector engineering. "We've moved from conventional card-rack, connector electronics to microelectronics that are closely aligned to the detector elements."

In the final assembly in the scanner's gantry, technicians place the ADC boards, sandwiched together in modules, in an arc-shaped mechanical card rack. An array of digital-interface (DIF) boards, which power and control the ADC boards, occupy another rack. A micropositioning system on the gantry aligns the x-ray input of the scintillator to a collimation system that defines the direction and dimensions of the x-ray beam. The entire assembly spins at 0.35 s per rotation, resulting in forces of 22 g on the detector boards.

Fast-paced design and test

Ensuring the quality of this network of boards on the V-Res detector demanded cooperation among members of a global engineering team. About 20% of the team was involved in building test fixtures, designing and performing tests, and writing software code for boundary-scan, in-circuit test (ICT), and custom testers, according to Jean Marc Delplanque, the engineer in charge of design for manufacture. His group mapped out the test strategy for the detector boards and designed the process flow for board manufacture. They also built custom testers, both for GE's internal manufacturing and for outside suppliers.



The ADC board undergoes a test journey in manufacturing that begins with x-ray and automated inspection in the surface-mount stage and ends with a functional test of two ADC boards sandwiched together in a module. More tests await when the module is mated with other detector components.

TIM EVANS

Jeff Kautzer, manager of CT detector engineering, explained that the GE team is relying more on x-ray inspection to handle the tighter electronics packaging on detector boards.

Delplanque noted that the complexity of the VCT's electronics was four times that of the previous product, and the design and test teams wanted to boost the reliability compared to that of previous scanners with no increase in cycle time. "The important thing is that we designed our tests and manufacturing processes from the start based on the needs of the product—not on our organizational structure," he said.

With the VCT's design fixed by early 2003, the engineers responsible for the ADC and DIF boards found themselves testing prototype boards to weed out problems as early as possible, while at the same time ramping up the tests that would be needed for volume manufacturing. "I used to be a design engineer, so I know that getting early feedback from test is critical to getting the design right," commented David Sallis, component engineering and test manager at GE's Global Electronics Center (GEC), a sister facility in Milwaukee where the VCT's detector boards are manufactured.

Journey to reliability

A look at the test roadmap for the ADC boards demonstrates the company's commitment to provide as much critical feedback as possible. The journey begins at the surface-mount level, where GEC will soon introduce automated online inspection machines to assess solder-joint quality during the paste-printing process. To ensure the board electronics meet IPC Class 3 manufacturing standards, GE uses

Agilent's 5DX x-ray system to inspect solder joints for voiding and other defects.

"Because of the [VCT] system's high-density electronics, including micro-BGA packaging, we are using x-ray more and more in manufacturing," said detector manager Kautzer.

After the cleaning and washing stages, boards undergo in-circuit tests on an Agilent 3070 bed-of-nails system. Next, the engineers perform a functional test on the ADC board using a custom tester that accommodates eight boards. This test involves operating the ADCs at their expected frequency rate and under controlled temperature. The tester measures a dozen critical-to-quality parameters, including noise levels, leakage, offset, and integral and digital nonlinearity.

With its 64-channel capability, the LightSpeed VCT can produce high-resolution, 3-D images of most organs in 1 s, the heart in 5 s, and the entire body in 10 s.

Explained Delplanque, "This is a very important test because you are measuring parameters that you cannot measure effectively later on. Repairs also can be made much more easily at this stage, compared to later on in the process, when the boards are sandwiched into a module for another functional test."

The GE engineers also perform extensive accelerated-life and stress-screening tests on the boards, both at the prototype and final manufacturing stages. For example, prototype boards were tested in Thermex-Thermatron ovens at temperatures ranging from –40°C to +125°C for 8 hrs. The normal operating temperature of the CT scanner is +15°C to +45°C.

Following stress screening and another functional test, the ADC module faces still more tests when it is mated with the diode assembly and scintillator pack as a complete subsystem. At this stage, the engineers perform at least a dozen tests in a clean room, using a digital modular tester and a slave x-ray source. They monitor the conversion of x-rays to electronics and the optical interface between the scintillator and the photo diode. "Anywhere that you have energy conversion going on calls for more elaborate and more difficult tests," explained Kautzer.

Next, the assembly goes to system manufacturing, where it is loaded onto a gantry equipped with an x-ray tube and a generator. The detector array is optically aligned with the collimation system, and the engineers can test dynamic images, instead of just the static images tested in the earlier digital module test. More tests follow on the entire CT machine in lead rooms at the Waukesha facility, including tests of the spatial and temporal resolution of the system.

Rewards of boundary scan

The test team also made use of boundary scan—using Goepel's Cascon software—for prototype development of the detector's critical boards. "About 30% of our boards have large digital content suitable for boundary scan," said Bobby Compton, the engineering manager who introduced the technology to the VCT platform team. "Within a few days, we were able to get a quick and easy boundary-scan test going, compared to the 10 weeks it can take to build an expensive ICT fixture."

On the DIF boards, for example, the boundary-scan tests checked for functionality and for electrical faults in the onboard power supplies. Without the boundary-scan system, there was a 67% yield of functional DIF boards during the prototype stage, where the engineers used scopes, probes, meters, and logic analyzers to prove out the design. But when they used x-ray inspection and boundary scan, the yield jumped to 98%.

"This was a real eye opener that CT engineering really loved," recalled GEC test manager Sallis, "because they now had a much larger volume of boards to work with. The result was a highly accelerated development process."

Added Russ Hum, the lead development engineer for the VCT's data-acquisition system: "We went from hours de-


TIM EVANS

With the project's tight cycle time, the team needed to spot problems as early as possible. Here, engineers Brian Breuer (front) and Steve Woloschek perform fault-seeding tests on detector boards.

bugging a board with bench instruments to just minutes with boundary scan."

Compton and his team say that boundary scan can also play a role in volume production. Team member Larry Beine built a fixture that can simultaneously test four cards used to reconstruct the CT images. "The pin density on these boards is high enough that it is very difficult to design an ICT fixture that can thoroughly test it," explained Compton.

A bit of home brew

Examples abound of such test ingenuity throughout the VCT project, which helped speed design and curb costs. For instance, in the development of the DIF boards, Hum's team built a PC-based simulator that allowed engineers to hook up the data-acquisition system to the ADC boards to take simulated scans and collect data. To test the regulators on the DIF boards, Beine used a small ADC chip on the board to measure voltages, eliminating the need for an additional test circuit setup outside the board.

And while the ADC module team had to build custom testers for several key stages in the manufacturing process, the engineers used the same software throughout, changing only the configuration files. Among the key components of these testers: a voltmeter, a PXI chassis and PXI boards, a CAN interface, and a PC.

"These aren't simple Class 1 boards we are dealing with," noted ADC module team leader Joe Block. "The delicacy of the measurements at the front end—in picoamps—challenges us to design testers that are effective and rigorous at those levels so that these boards are highly reliable inside a CT scanner." Such reliability is crucial to the functioning of the scanner. If even one of the 1024 A-to-D channels in the CT's detector array malfunctions, the image is often unusable.

The GE engineers also had to find ways to keep from drowning in all the test data collected during board development, pointed out Delplanque. The solution: save detailed test data on failures or marginal performance, while relying on overall statistics to track the results of passed components. Engineers also designed a visualization tool that lets manufacturing quickly identify patterns in board failures.

An engineering triumph

By all accounts, such innovative test work played a major role in the LightSpeed VCT's success. Despite the need to coordinate numerous design and test teams involved with multiple subsystems, the cycle time for the VCT was much faster then it was for the first LightSpeed CT introduced in 1998, noted Gary Strong, the lead engineering manager on the project.

Recent articles in publications such as *Radiology Today, Popular Mechanics,* and the *Wall Street Journal* have heralded the technical advancements of the machine. And within GE itself, the scanner has garnered the company's coveted "imagination breakthrough" designation. "The word we are getting from within the company is to make more of these machines," said manufacturing test engineer Gary Schilling. "It's a big hit with customers."

Brian Kost, who manages the engineering effort for all of GE's CT scanner products, traces the VCT's success to its ability to answer the needs of the medical community—most notably, greatly enhanced imaging of the heart. "It's a great product to be associated with," said Kost, "and we couldn't meet the demand that we are getting right out of the chute without the critical role of test. It helped us catch problems early in the process, giving us the assurance in final assembly that we are building a quality product." T&MW

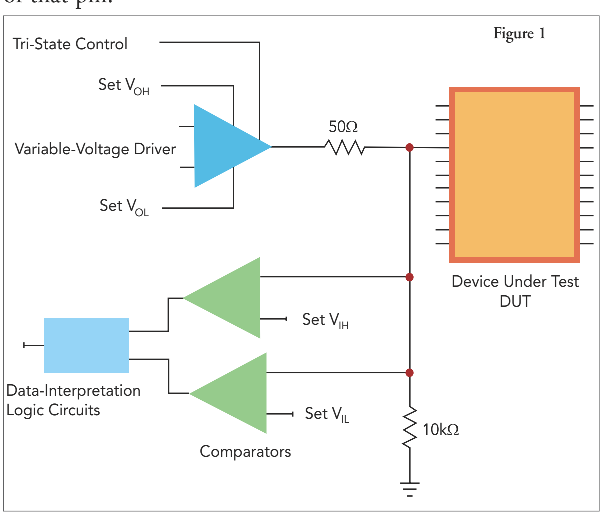
THE DATA DETECTIVE

Digital Data Hits Highs and Lows

When testing digital circuits, engineers stimulate inputs and monitor outputs to determine whether or not devices or circuits work properly. Thankfully, software can take a design and create a pattern, or vector, of 1's and 0's that test equipment can automatically apply to digital inputs. A mismatch between a device's actual and expected output indicates a fault.

Many manufacturing faults of digital components fall into one of the following categories: open circuits, short circuits, or stuck-at faults. The latter group divides into stuck-at-1 or stuck-at-0 faults, which means an output remains "stuck" at a logic-1 or a logic-0 level.

Most equipment used to test digital circuits includes both a voltage driver and comparators for each channel, as shown in the figure below. These pin electronics let test engineers stimulate a device's digital input as well as monitor the state of that pin.



The circuit above, similar to those found on the National Instruments NI-655x waveform-generator/analyzer cards, includes independent stimulation and measurement electronics that operate simultaneously. Each pin requires its own driver and comparator circuit.

The variable-voltage driver shown in the figure will generate a high output voltage (V_{OH}) or a low output voltage (V_{OL}) to produce a logic-1 or a logic-0 at the input of a device under test (DUT). The driver circuit also can present a high impedance to the DUT, in effect disconnecting the driver portion of the pin electronics from the circuit. Programmable V_{OH} and V_{OL} levels let this circuit drive ICs in many logic families. The 50-Ω series resistance at the driver's output enhances signal integrity.

Measurements at the driver's pin involve two comparators, one that compares the DUT's output voltage to a low acquisition voltage (V_{IL}) and another that compares the DUT's output to a high acquisition voltage (V_{IH}). (Software will preset these voltages, depending on the tests an instrument requires.) Logic circuits connected to the comparators in the pin electronics determine whether the DUT produced a valid logic 0 or logic 1. In the event of a fault, this logic also can determine if the DUT has produced an invalid output between the preset V_{IL} and V_{IH} levels. The comparator circuit provides a known input impedance—a 10-kΩ resistor that connects to ground. Note the comparator circuits operate independent of the voltage driver, so the digital test equipment can simultaneously stimulate a pin as well and measure the voltage on it.

To test a device, digital test equipment can apply a "marching 1" pattern—1000.., 0100.., 0010.., and so on—to a DUT's pins. The tester monitors the DUT's pins to ensure the detected pattern matches the output pattern produced by the driver electronics. If a marching-1 pattern produces logic 1's at two or more pins, a short may exist between those pins. Likewise, if the driver applies voltage and not enough current flows—as detected by the comparators—the circuit may have an open. (Tests also may use a marching-0 pattern; 0111.., 1011.., 1101.., and so on.)

Stuck-at faults usually appear when a conductor shorts to a power-supply (Vcc) or ground connection. During a marching-1 or a marching-0 test, for example, a stuck-at pin will appear as an extra 0 or 1 in the pattern. Generally, no amount of stimulation will change the state of a stuck-at pin.

Don't worry about constructing pin electronics—companies offer them for buses such as PXI and VXI, and they come as part of some automatic test equipment (ATE). Companies also offer test-development software.

The Chips are Down

Chris received the first batch of digital ICs he designed to operate at a custom voltage. Much to his dismay, initial tests show no chips work. Chris plans to use a digital I/O board to determine whether the problems exist in his design or in the silicon.

To help Chris test the chips and discover the problem, go to

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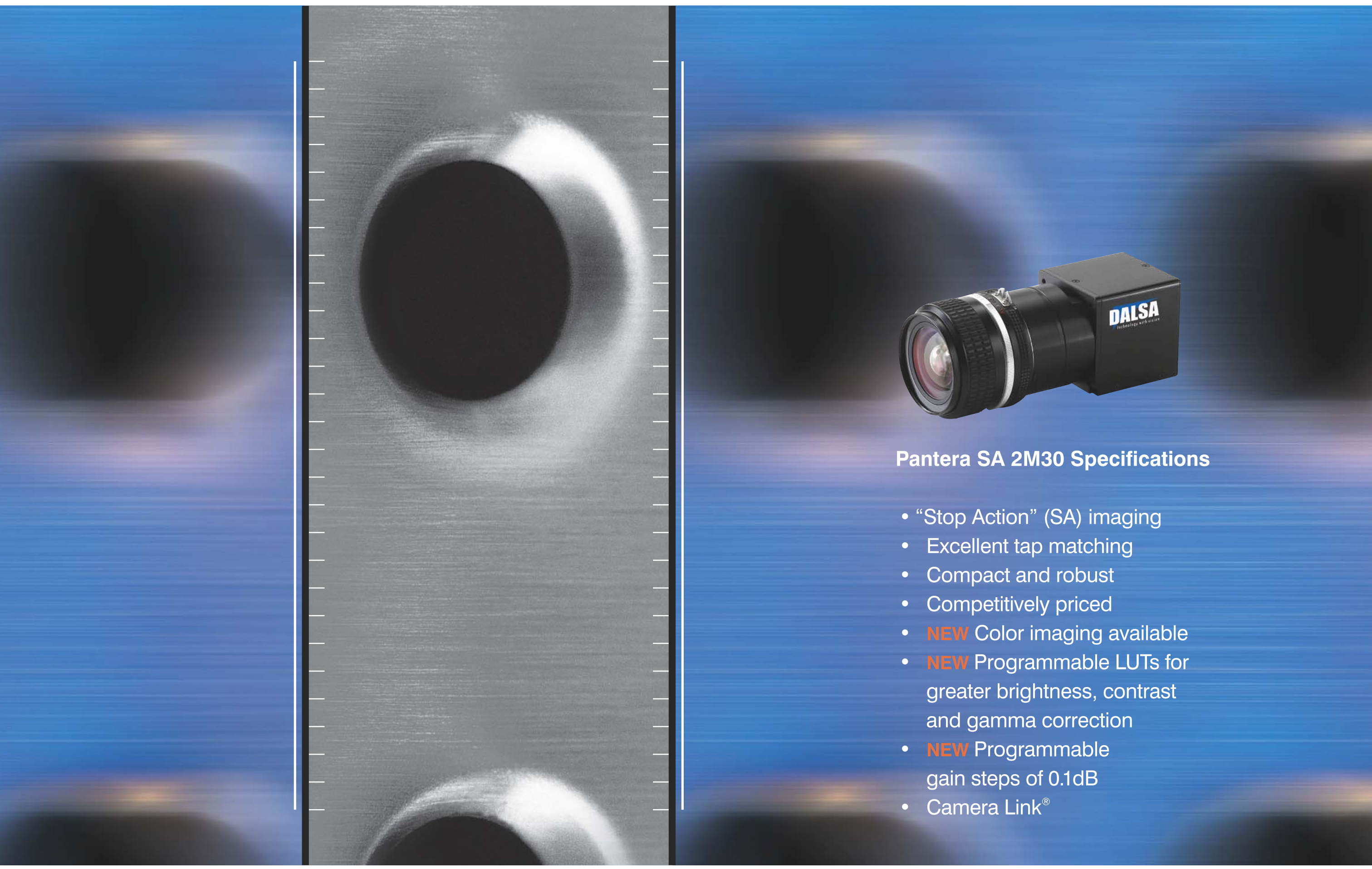

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TEST REPORT

PARTS MARKING

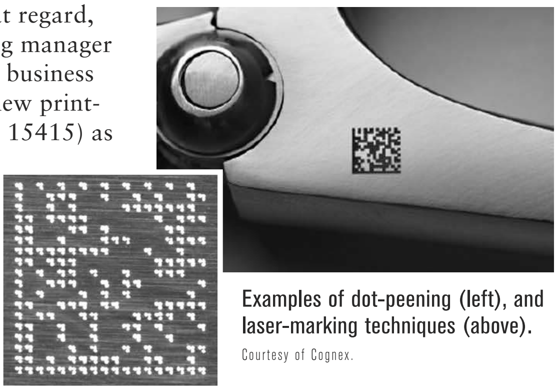
Keeping track: Evolving standards

Steve Scheiber, Contributing Technical Editor

The move toward tracking parts by marking them directly rather than by relying on labels that may come off during manufacturing is gaining momentum. In fact, the US Department of Defense (DoD) MIL-STD 130 now requires manufacturers to mark parts with a unique identifier. Concurrent with this trend, one-dimensional bar codes are being replaced by two-dimensional Data Matrix codes—a collection of black and white dots or squares arranged in a rectangular pattern—that convey more information in less space.

Initially, companies employed direct part marking (DPM) primarily for internal process and inventory control, so the meaning of the marks differed from company to company. As the use of the DPM technique left the manufacturing plant and moved into the supply chain, an open-standard specification arose to ensure readability and avoid misinterpretation of codes as parts passed from one company to another.

Direct-part marks must be both verifiable and readable by vision and inspection systems. In that regard, says Carl Gerst, marketing manager for Cognex's ID Products business unit in Natick, MA, the new print-quality specification (ISO 15415) as well as the original Data Matrix specification (ISO 16022) made some unfortunate assumptions about DPM verification. The specifications assumed that—like paper-based inked bar-codes—DPM codes would predominantly consist of high-contrast, well-formed square cells of equal size.



Examples of dot-peening (left), and laser-marking techniques (above).

Courtesy of Cognex.

Techniques challenge standard

When manufacturers turned to different marking techniques, such as lasers, electrochemical etch, and dot-peen, however, the standards proved less than successful. Laser marks on metal are more likely to appear as gray-on-gray than as black-on-white. As a result, verification systems that base their pass/fail decisions on tight contrast measurements may fail DPMs that readers can read with little difficulty.

In addition, dots may be square or round, depending on the marking technique: Dot-peening tends to produce round marks, ink-jet and laser marks can be round or square, and electrochemical etching tends to produce square marks. Also, with the dot-peen technique, the dots are typically smaller than the blank spaces around them. Standards must take these factors into account.

Although the ISO is responsible for issuing the standards, the organization does not create them. That role falls to the Association of Automatic Identification and Mobility (AIM; www.aimglobal.org). Gerst and representatives of other companies have been working with AIM's Technical Steering Committee to revise the Data Matrix standards along more practical lines.

Revisions on the way

Gerst expects the revisions will be released and implemented sometime in Q3. He also anticipates that these standards will eventually be incorporated into the next revision of MIL-STD 130. Even companies that do not work directly with the DoD will likely adopt the standards.

The good news about the evolving Data Matrix standards is that the changes are being orchestrated from the bottom up—that is, by users of the standards who have assessed their limitations. The resulting changes will serve all interested parties better than standards developed in an ivory tower by people without the day-to-day practical experience. □

INSIDE *this issue*

EDITOR'S NOTE

Inspection? What's inspection?

Steve Scheiber, Technical Editor

Putting out this test report requires drawing the boundaries within which to work. Where does testing stop and inspection begin?

Identifying automated optical or x-ray techniques as inspection does not require much of a stretch. Ditto classifying functional or system test or "hot mock-up" as test. But some techniques fall into a gray area.

Infrared analysis looks for hot spots on a printed circuit board. Most commonly used to detect shorts on a board (very) briefly under power, subtler versions can examine a board in normal operation, comparing its thermal signature to that of a good board. In that sense, the technique resembles functional test more than inspection. Nevertheless, because it tests by "looking" at the board–even a board in operation–I classify it as inspection.

Some moving-probe testers include cameras for more accurate x-y positioning. Those cameras can also perform rudimentary inspection—especially presence/absence inspection. Because these systems' primary function is test, however, I lump them in with the testers.

The ultimate goal of all the techniques is the same—to ensure that a circuit works—so making such divisions may seem pointless. But finding an optimum engineering solution generally means breaking large problems into manageable pieces. Establishing these distinctions, however arbitrary, helps to focus our attention on optimizing each process step. □

Contact Steve Scheiber at sscheiber@aol.com.

NEWS

Dalsa licenses image sensor technology

DALSA HAS announced a technology licensing agreement with Philips Electronics. Under the license, Dalsa will use Philips patent rights, know-how, and product and prototype device designs relating to CMOS imaging technology.

This agreement follows Dalsa's creation of a new CMOS Business Unit earlier this year, and Dalsa says that the access to Philips' CMOS technology will give it an even stronger base from which to launch new products. The initial focus for the new CMOS group, and for the application of the Philips' technology, will be in the professional and high-volume industrial markets.

Sawas Chamberlain, CEO of Dalsa, said, "I am very pleased to have access to Philips' world-leading CMOS technology for image sensor products and to bring on board the team that helped develop it. This will allow us to make use of the CMOS technology and product designs almost immediately and well into the future." www.dalsa.com. □

Cognex, Lockheed promote ID products

COGNEX HAS REPORTED that it will work with Lockheed Martin to promote products that will help Department of Defense contractors meet new government requirements for unique identification of parts. The company says that the DoD Unique Identification (UID) Compliancy Initiative requires that every piece of equipment purchased by the DoD with a value greater than $5000, or that requires serialization, be marked with a unique 2-D matrix code.

Cognex manufactures ID readers designed to verify 2-D Data Matrix codes on a variety of surfaces. Lockheed Martin supplies I-Guides, a software application that manages UID-related data, creates a process audit trail, and ensures that the supplier's process meets DoD policy requirements. Used together, the two company's products can help contractors meet the DoD identification requirements.

"This agreement enables Cognex and Lockheed Martin to approach customers with a simple-to-adopt solution for meeting Department of Defense compliancy requirements," said Justin Testa, senior VP of ID Products for Cognex. "As a result, customers can get state-of-the-art technology, and avoid the cost of reinventing the process internally."

"UID compliancy requirements represent a big change for Defense Department suppliers, and this agreement can make those changes easier for suppliers and accelerate the success of the Defense Department's UID program," said Richard Erickson, program manager for I-Guides at Lockheed Martin Maritime System & Sensors' Tactical Systems line of business. www.cognex.com. □

Calendar

International Robots & Vision Show
September 27–29
Rosemont, IL
Sponsored by: Automated Imaging Association and Robotic Industries Association
www.machinevisiononline.org

Vision 2005
November 8–10
Stuttgart, Germany
Produced by: Messe Stuttgart
www.messe-stuttgart.de/vision

AIA Business Conference
February 1–3, 2006
Orlando, FL
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X-RAY INSPECTION

Closing the gap between AXI and semi-automated systems

Boris Mathiszik and Holger Roth, phoenix|x-ray Systems + Services

Manufacturers of industrial x-ray equipment judge the quality of an x-ray system by the images it produces and the information derived from those images. While the hardware is certainly a key to system quality, it is software that differentiates the many low-cost manual systems from the mid-priced semiautomated and higher-priced automated systems.

The line that separates these inspection classes, however, is beginning to blur. Semi-automated machines now include sophisticated image-processing software once found exclusively on automated x-ray inspection (AXI) systems, and they can replace AXI systems in many applications.

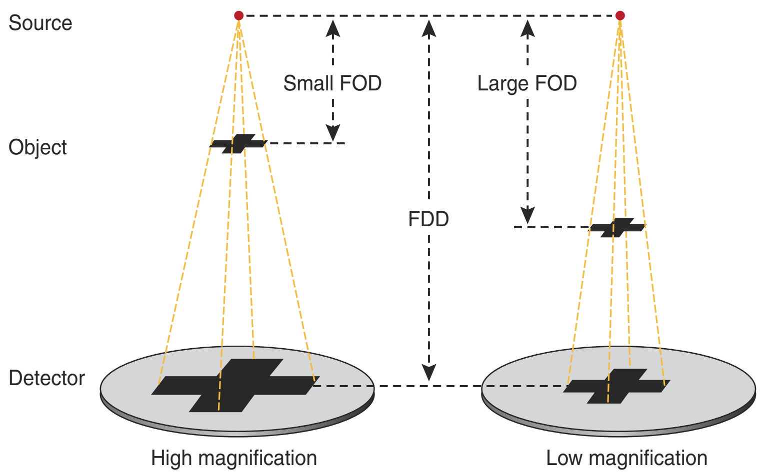

Fig. 1 The geometric magnification of an x-ray shadow microscope equals the focus-to-detector distance (FDD) divided by the focus-to-object distance (FOD).

Obtaining quality images

In electronics imaging, magnification and focal spots are often misunderstood. While many manufacturers quote the software magnification (or pixel magnification), it is a system's geometric magnification that places limits on image quality (**Figure 1**). Most x-ray machines achieve high magnification by moving the target, the detector, or both, which takes time. Thus, AXI machines often sacrifice magnification to minimize test time.

At higher magnifications, the focal spot size of the x-ray source limits resolution and causes image blurring or a "penumbra" effect. The image on the left in **Figure 2** represents an image from a large-spot size x-ray tube architecture that can resolve images down to a few microns, a technology that was introduced about 20 years ago. Newer designs improve on that performance by an order of magnitude. By manipulating additional lenses and apertures to produce a converging beam hitting the output tungsten target, the resulting tube provides an extremely small focal spot that reduces the penumbra effect (right side of Figure 2). Incorporating this capability into semi-automated x-ray systems allows those systems to meet customer demands at a lower cost.

Achieving a high-quality image also requires a good detector. The quality of the detector—even for the latest digital types—primarily affects image contrast. Other techniques that aid in capturing clear images include tilting the target and a technique that we at phoenix|x-ray call oblique view at highest magnification (OVHM). Although effective, tilting takes time for switching to the oblique angle and realigning the often shifting field of view. Our OVHM technique allows full off-axis detection while keeping the target close to the focal spot. We find that the technique delivers high-quality images in a reasonable time with no loss of magnification.

Software

Software and image-analysis tools are becoming the differentiating features that separate less than $100,000 x-ray systems from semi-automated and AXI machines. Fast, effective image-analysis software has more impact on speed, accuracy, and repeatability than any other aspect of the system. Software can also blur performance differences between AXI and semi-automated tools, making automated handling the primary difference.

Whereas most low-cost semi-automatic x-ray machines include limited software packages, many of the tools used on AXI and automated optical inspection (AOI) machines are migrating down to the mid-priced semi-automatic systems and are changing the way these machines are being used. Suppliers of semi-automated x-ray systems have begun to add BGA defect coverage ranging from ball presence/absence and bridging detection to void analysis, diameter measurements, roundness checks, and automated wetting analysis. For IC packaging applications, the tools perform automated void detection for conductive and nonconductive die attach, solder-bump inspection, wire-bond integrity checks, and wire-sweep measurements.

In the latest software packages, standard BGAs, fine-pitch BGAs (FBGAs), and chip-scale packaging (CSP) device libraries allow users to teach inspection systems to recognize

Closing the gap • from page M5

component layout, proper solder diameter, and acceptable gray levels with minimal setup time. Many packages even offer default threshold values, reducing setup times even further.

Like AXI and AOI systems, semi-automated machines are using image-processing software packages to import PCB CAD data, reducing setup time. The software integrates automated inspections, automated pass-fail decisions, and data links to rework or paperless repair stations.

Defect coverage

Manufacturers typically use semi-automatic x-ray inspection equipment in two ways—either as manual real-time failure-analysis tools in laboratories or as quality-assurance tools in production. Some semi-automatic x-ray systems now incorporate AXI tools for production applications.

For BGA, CSP, and flip-chip applications, automated inspection using oblique views has increased defect coverage. AXI based on oblique viewing provides two advantages. First, angled views and sample rotation allow programmers to maximize signal-to-noise ratios on double-sided boards where signals from the other side of the PCB blur or deform the signal of the primary inspection target. Second, oblique viewing enables automated wetting inspection.

Customers of semi-automatic x-ray equipment continue to ask vendors to extend their automated defect coverage beyond standard BGAs. Typical applications include inspection of gull-wing devices such as quad-flat packs (QFPs), plated-through holes (PTHs), and connector pins. Adding such measuring techniques enables new customers to increase the automated defect coverage without buying a fully automated machine. Existing users can also take advantage of the new features at little extra cost. Unavoidable extra costs include acquiring the appropriate software modules, minimizing programming time, and potentially increasing inspection cycle time. The cost savings result from less rework and scrap in the field and from transferring test coverage from a later manufacturing and test process step to an earlier step—typically after reflow in the SMT process.

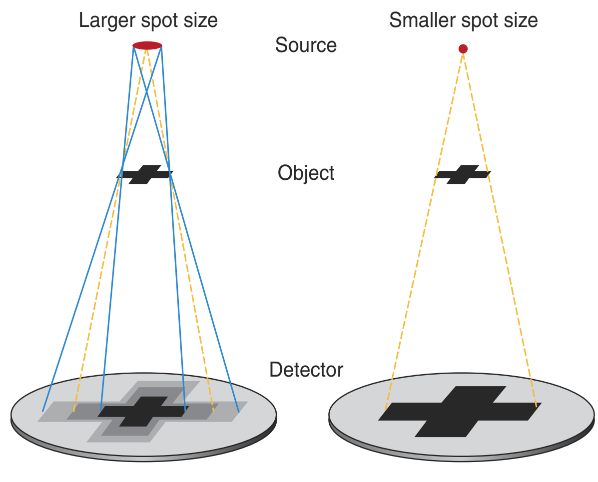

Fig. 2 Because of the penumbra effect, the size of the source limits the resolution of the image.

True submicron x-ray inspection systems have been the "holy grail" of the x-ray industry for many years. Yet, submicron x-ray tubes are unlikely to replace large-spot tubes for all inspection applications in all industries. Lower resolution systems will still be used to inspect large, dense objects, because their ability to create a large x-ray flux cannot be duplicated with submicron sources. □

Boris Mathiszik is VP of phoenix|x-ray's East Coast division. He has been involved in product management for AOI and x-ray equipment for the past 10 years. bmathiszik@phoenix-xray.com.

Dr. rer. nat. Holger Roth is applications manager at phoenix|x-ray Systems + Services in Wunstorf, Germany, and is in charge of the company's inspection service laboratory in Stuttgart. hroth@phoenix-xray.com.


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AUTOMATED OPTICAL INSPECTION

Meeting the lead-free inspection challenge

Steve Scheiber, Contributing Technical Editor

The movement away from using lead-based solders presents challenges to board manufacturers. Not only must they find a solder that offers properties as close as possible to those of lead solder, but they must also find new ways to test their products and verify their circuits. Automated inspection offers one answer to the second problem.

Regulations in Europe and China require the removal of all leaded components and solder in certain electronic products sold there by July 1, 2006. Other countries—including the US—are expected to follow suit.

The new regulations do not cover all products. Exceptions include telecommunications network infrastructure, medical products, and defense and aerospace systems. Nevertheless, high-volume products such as personal computers, televisions, DVD players, and cellular phones must conform. Stig Oresjo, senior test strategy consultant with Agilent Technologies, estimates that the regulations will cover 60–70% of all boards sold into the regulating countries (Ref. 1).

Although companies might like to make the transition by following Path A in **Figure 1**, limited knowledge of the effect of lead-free solder on the process and the dearth of lead-free components will make that approach impractical. Industries forced to go to lead-free will probably follow Path B, incorporating lead-free solder and adding lead-free components as they become available.

Path C will apply more to exempt industries, where companies will continue to use conventional tin/lead solder but will adopt lead-free components as parts makers introduce them. Companies that make both covered and exempt products may elect to make all their products lead-free to avoid maintaining two different manufacturing processes, inventories, and test and inspection strategies.

New alloys, new failures

After experimenting with metals, the electronics industry has settled on a range of alloys consisting mainly of tin with a few percent silver and less than 1% copper. These solutions prove less than perfect, however. Board manufacturers can expect more defects, at least at first. Lead-free solder melts at 217°C compared to 183°C for its predecessor. The higher temperature required for soldering and rework will subject components and substrates to additional stresses that will reduce their reliability.

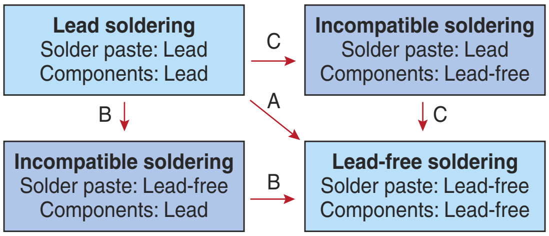

Fig. 1 While most manufacturers would prefer to make the transition to lead-free manufacturing by following Path A, they are more likely to follow Path B. Manufacturers not governed by the regulations may follow Path C. Courtesy of Agilent Technologies.

Oresjo contends that because of the higher temperature, manufacturers may permit fewer repair attempts after a failure. "Shotgunning" a board after a functional-test failure may prove damaging as well. Both procedural changes will likely mean more scrap.

Also of concern, thanks to its metallurgy rather than its melting temperature, is that the new alloy exhibits lower wetting characteristics compared to lead solder. Wetting of molten solder determines how well it covers pads and device leads, as well as the shape of the resulting solder joints. Sufficient wetting also helps slightly misplaced components to adjust themselves by floating a little on pads during reflow.

Wetting forces during reflow tend to draw tin/lead solder paste back to pads, reducing the likelihood of shorts caused by solder bridges. Lead-free boards won't react in the same way, and will therefore tend to have more shorts. Also, lead-free wave-soldering may produce insufficient barrel fill on boards with through holes.

Because some manufacturers have started to conform to the regulations, the industry already has data on lead-free manufacturing. **Figure 2** shows results from one manufacturer who makes two similar boards—one using tin/lead solder and the other lead-free. Each board contains about 1300 components and about 3000 solder joints, including BGAs, gull-wings, and SMT connectors, with the smallest component an 0402 with a pitch as low as 20 mils. The data cover 85,000 leaded boards and 60,000 lead-free. The figure includes only fault types affected by the change.

The greatest increase appears in tombstone faults, with significant increases in solder opens and chip misalignments. Contrary to expectation, these data show a decline in defect rates for solder bridges and shorts. Oresjo suggests that this result may be mere coincidence or may result from the close attention paid to the manufacture of this board by experienced engineers who kept the process under tighter-than-normal control.

Impact on inspection

From a process perspective, making lead-free boards will require more accurate solder-paste deposition to avoid inadequate pad coverage. Al-

Lead-free inspection • from page M9

though inadequate pad coverage would not generally be flagged as a defect, a fixture nail might miss the solder during in-circuit test and hit bare copper. Because solder provides better nail contact than copper does, the resulting tests may generate false failures. Similarly, the inability of components to correct themselves during reflow will mean stricter calibration of pick-and-place machines.

To deal with these issues, Oresjo recommends performing automated optical inspection (AOI) at post-paste and post-placement. Post-paste AOI will ensure adequate solder-pad coverage and allow for inexpensive correction. Correcting inadequate or inconsistent solder volume before adding components will dramatically reduce solder-related problems later on.

Post-placement AOI would find misaligned components. With leaded solder, this step is often skipped precisely because the devices may move during reflow. Since movement is less likely with lead-free solder, a post-placement defect will remain after reflow, and repairing it at the earlier step proves less expensive.

Because of its lower wetting properties, lead-free solder is also less forgiving of slightly bent device leads, which may contribute either to actual performance faults or reliability (field) failures. Again, an additional inspection step can identify these problems even if the circuit functions properly.

Unlike other test methods, AOI can handle lead-free alloys with little adjustment. The new alloy is less shiny than the leaded version, joint shape will differ somewhat, and lead-free joints are grainier than with traditional solder, but such differences are relatively minor. Oresjo cites a study conducted by the National Physical Laboratory in the UK on six AOI systems. It concluded that the AOI step will perform as well as before with few modifications.

The effect of the higher defect levels that lead-free solder will likely create, however, may prove more problematic. Manufacturers already contend that AOI generates too many false calls, especially false failures. With a rise in board failure rates, such complaints will likely become more insistent, even if the inspection results are as reliable as they were before.

Production bottlenecks may present a problem. Even cursory AOI takes time, and an increase in inspection efforts to cope with rising defect levels may mean inspection times that exceed the permissible beat rate. In addition, since a manufacturer may perform AOI at more places in the process, this problem may occur at more points as well.

Reliability concerns will increase the need to perform post-reflow inspection. Lead-free solder is more brittle than tin/lead, so even if a circuit functions in the factory, there is no guarantee that shipping it to the

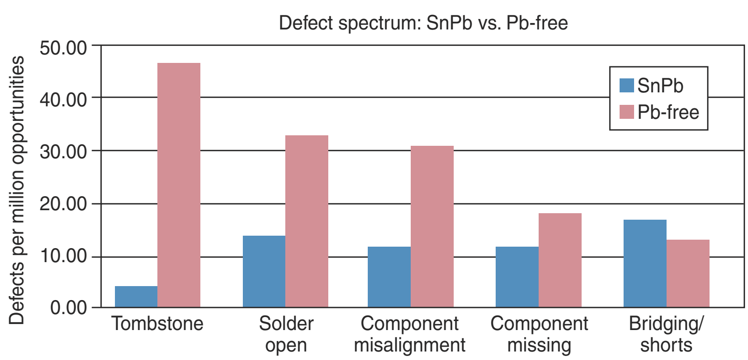

Fig. 2 One contract manufacturer reports these defect levels for high-volume PCBs; the results cover 85,000 leaded boards and 60,000 lead-free boards. Courtesy of Agilent Technologies.

customer will not cause a failure. To handle BGAs and other hidden nodes, automated x-ray inspection (AXI) will likely become the post-reflow inspection method of choice.

Lead-free solders offer less impedance to x-rays. Recalibration of AXI equipment can compensate. If both leaded and lead-free boards of the same type come down the line, for example, merely tweaking gray levels in the test program may suffice.

Analysis of inspection results offers side benefits. Diligently feeding results back into the process can permit improvements that minimize future defects. When manufacturers first turned to no-clean processes several years ago, defect levels in many places rose by an order of magnitude. As the industry gained experience in how the process differed from its predecessor, defect levels began to drop until they reached close to the level where they had stood before the change. Oresjo suggests that lead-free manufacturing will likely follow a similar pattern.

Making the transition

Before addressing the issues raised by lead-free manufacturing, Oresjo recommends looking carefully at your current defect levels and fault spectrum. Understanding where you are today will help you manage the transition. He also suggests switching over only one manufacturing line at a time so you can more easily track and solve problems. Each line switchover should then proceed more smoothly than the last, and the entire migration will prove as painless as possible. □

Reference

1. Oresjo, Stig, "Test and Inspection as part of the lead-free manufacturing process," Proceedings of the ECWC 10 / APEX Conference, February 22–24, 2005.

PRODUCTS

Programmable smart camera

The Iris P300H programmable smart camera incorporates a monochrome 640x480 one-third-inch CCD sensor and captures data at 100 frames/s. It is designed for high-throughput inspection applications that demand simple analysis or processing of images. The camera features software API for image analysis. *Matrox Imaging, www.matrox.com.*

Intelligent cameras

The new Impact T26 and T27 intelligent cameras are supported by PPT Vision's Inspection Builder software, which comes with algorithms for pattern matching, blob analysis, subpixel gauging, and character inspection. The T26 incorporates a 1280x1024 CMOS high-resolution imager; the T27 offers a 1600x1200 CCD imager. *PPT Vision, www.pptvision.com.*

Imaging chain for x-ray systems

Feinfocus has announced the HDX-ray 16-bit imaging chain for its FOX x-ray inspection systems. The 2.6-Mpixel imaging subsystem features more than 65,000 gray scales with selectable frame rates from 1 to 30 frames/s. HDX-ray is available on all FOX systems or as an upgrade. *Feinfocus, www.feinfocus.com.*

Wafer reader

The In-Sight 1721 wafer ID reader tracks semiconductor wafers through the manufacturing process. Slimmer and faster than its predecessors, it still maintains mounting and functional compatibility with them. Cognex says the In-Sight 1721 reads wafer marks that have been affected by process effects such as CMP, edge beads, and copper metallization. *Cognex, www.cognex.com.*

ADVERTISER INDEX

Machine Vision & Inspection Test Report is published in four issues of *Test & Measurement World*

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U6

FEARS TEMPER CAREER SATISFACTION

ALTHOUGH SATISFIED WITH THEIR JOBS, TEST ENGINEERS WORRY ABOUT THE EFFECTS OF OUTSOURCING.

LAWRENCE D. MALONEY, CONTRIBUTING EDITOR

Most engineers love what they do for a living, but more of them are now asking, "Will the global economy take my job away?"

That's a key conclusion from a new *Test & Measurement World* reader survey on careers and salaries, as well as from interviews with engineers on the opportunities and frustrations of the profession.

Many engineers still view the test field as an attractive one, but they stress that it is more important than ever to keep pace with new technology and develop an appreciation for the business needs of their companies. "It's vital that engineers be proactive about their careers," said Michael Keller, a 30-year engineering veteran and director of the American Society of Test Engineers (ASTE). "You need to have a plan on where you want to be five years from now and begin taking the steps to get there, such as earning an MBA or a graduate degree in engineering or computer science."

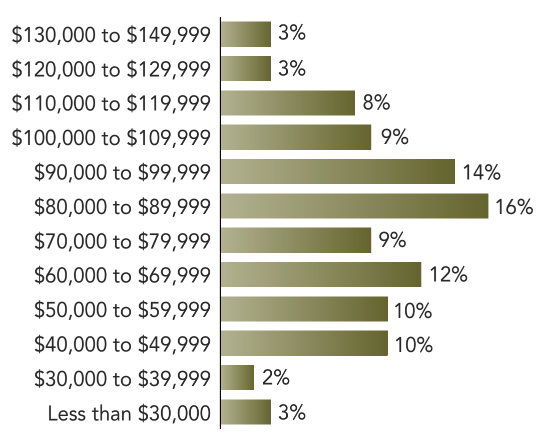
Rising pay, more responsibility

The *T&MW* survey reveals an average salary of about $78,700, with more than half of respondents reporting a salary of more than $80,000. Three quarters expect a pay hike this year, and the average expected increase is about 5%.

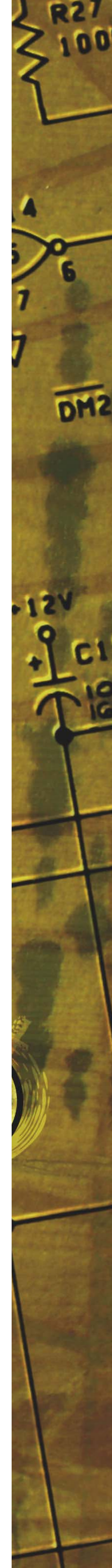
But along with good pay comes more responsibility, as companies quicken the pace of product development without a commensurate increase in the engineering ranks. The *T&MW* study finds 72% of respondents reporting an increase in the number of job functions they are being asked to perform. Time pressures and a growing number of projects also were cited as the top two job challenges.

Ray Worcester, who develops PCB fixtures for Tyco Healthcare in New York, said that with

Where do you stand on salary?



Source for all charts: 2005 Salary Survey, *Test & Measurement World*/Reed Research Group.



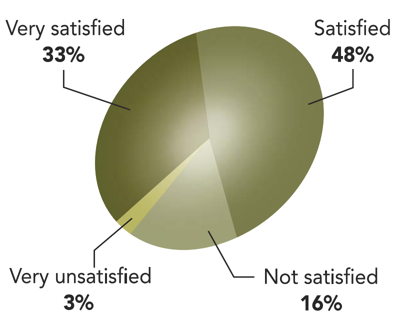
ENRICO VARRASSO

shorter design cycles, he has completed twice as many projects in the last six years as his predecessor did in a comparable period. Even working extra hours, he somehow found time to earn a master's degree in advanced technology, which includes subjects ranging from nanotechnology to the financial aspects of engineering.

"The biggest daily challenge that most engineers must deal with is being able to multitask," said Darcy Dement, a senior product manager at National Instruments. "That was something I struggled with as a new engineer six years ago." She noted that being able to prioritize among several projects can often present a bigger challenge than the technology itself.

With defense orders surging at Raytheon, engineer Bob Rassa agrees that it is a challenge to keep from overworking engineers and other technical staff. "Quality of life issues, such as the need to balance between work and family life, are a real concern," said Rassa, who also serves as the president of the IEEE's Instrumentation & Measurement Society.

Satisfaction with engineering career?



Duane Quam, a Minnesota engineer who develops manufacturing tests for JDS Uniphase, cited "working with new technology" and "having enough people to do the job" as two of the chief pressures he faces. "You need to be so much more efficient today," he said.

Even with increasing workloads, most engineers remain fairly content with their work. Our reader survey shows that 81% of respondents are either satisfied or very satisfied with their work. The three biggest contributors to job contentment: a feeling of accomplishment (41%), technical challenges (37%), and salary (31%).

"Creativity in test methods is critical to the success of every product, and it is important for organizations to understand and appreciate that," said Jeff Lewis, quality assurance manager for Arrow International, a Pennsylvania-based medical equipment company. "So the work environment itself plays a big role in job satisfaction."

An uncertain outlook

With the first of the huge baby boomer population turning 60 next year, medical companies like Arrow can look forward to rising business opportunities, which will benefit engineers. Also enjoying solid business: OEMs and their suppliers in commercial aircraft, off-road and heavy equipment, cell phones, and other consumer electronics. Boeing's orders, for example, were up 25% for the first four months of 2005, versus the same period in 2004, while Caterpillar is projecting at least a 35% jump in profits this year to a record $2.6 billion. Apple Computer, with its hot iPod product, enjoyed first quarter profits that were up 530% over the same 2004 quarter.

But other sectors of manufacturing—most notably automotive—find themselves reeling from foreign competition and, in the case of General Motors and Ford, internal problems as well. Add to that the movement of more manufacturing operations to China and the outsourcing of more engineering jobs to foreign countries, and it's no surprise to see a nagging sense of worry among many engineers. The reader survey finds job security as the biggest single concern of respondents.

"The globalization of the economy is producing a demand for cheaper and cheaper goods, and as a result, we are shipping our future to China," said Roger Fish, a 30-year engineering test veteran in Wisconsin. His company, Jefferson Electric, makes power transformers for factories and is feeling the pressure from lower-priced Chinese products.

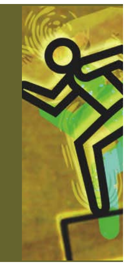
SNAPSHOT
of average respondent

AGE: 46

GENDER: Male
(96% of respondents)

SALARY: $78,700

EXPERIENCE: 18 years



Looking ahead, job growth for electrical and electronic engineers is expected to lag the average of all occupations, according to the latest Department of Labor forecast. The DOL's "Occupational Outlook Handbook 2004–2005 Edition" predicts that EE jobs will expand from 292,000 in 2002 to between 300,760 and 318,280 in 2012. That amounts to a projected increase in EE jobs of between 3% and 9%, compared to a 14.8% gain for the average of all occupations.

In summarizing the situation facing the EE field, the report notes: "Although rising demand for electrical and electronic goods, including advanced communications equipment, defense-related electronic equipment, and consumer electronics products should increase, foreign

What three factors have the greatest impact on your satisfaction with your current job?

Feeling of accomplishment	41%
Technical challenge	37%
Salary	31%
Advancement opportunities	24%
Job security	24%
Benefits	23%
Company's financial health	16%
Relationship with boss	16%
Relationship with colleagues	15%
Location	14%
Feeling of recognition	14%
Leading a team	11%
Workload	11%
Managing people	5%
Relationship with subordinates	5%
Company size	4%
Physical or ergonomic environment at work (positive or negative)	3%
Travel	3%
Other	1%

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competition for electronic products and increasing use of engineering services performed in other countries will act to limit employment growth. Job growth is expected to be fastest in service industries—particularly consulting firms that provide electronic engineering expertise."

Taking the initiative

With a tough job climate ahead, engineers see a need to become broader and more attuned to the business mission of their companies. "When technology was king, engineering led the pack," recalled Bob Durstenfeld with California's RAE Systems, which makes gas and radiation detection instruments. "Now, it is all about satisfying the consumer, and marketing plays a far bigger role." Because of this trend, Durstenfeld urges engineers to develop a "public persona" and learn to work more closely with customers.

AT Net Test, a Utica, NY, firm that makes equipment to test fiber-optic components and networks, Erik Wend agrees that engineers need to get broader in their outlook. "It can be as simple as being willing to do a white paper that will benefit customers," he said. "Such activities may seem like a distraction from your engineering duties, but they will make you more valuable to your company."

Dement of National Instruments also said that successful engineers need to have a blend of technical and business sense and be able to distinguish the features that are essential for a product, versus those that are tangential. "Today, it's not enough to be a great engineer," she explained. "You need to have an eye for business as well. The people who learn to do both become the real superstars."

What three factors do you think are most important to an engineer's career advancement?

Leadership in solving tough engineering challenges	64%
Ability to complete test projects on time and within budget	50%
Ability to function as a team player	49%
Communication and presentation skills	47%
A flare for creative ideas	32%
Demonstrated talent for managing others	29%
Superior computer and programming skills	12%
Other	4%

What's the best way to get plugged into the business issues and corporate culture of your company? "Find a good mentor," advised Lewis of Arrow International. He also puts great stock in the development of "emotional intelligence," as described by Daniel Goleman in his best-selling book, *Emotional Intelligence: Why it can matter more than IQ.* "You may be getting the desired results from your tests, but you have to be able to communicate these findings to others, and that plays into the whole teamwork theme."

In the *T&MW* survey, respondents placed "ability to function as a team player" and "communications and presentation skills" in the top four factors needed for career advancement. They also cited "keeping current on technology" as their second biggest career concern, indicating a need for continuing education, if not a formal advanced degree. "If you go for a graduate degree, you'll not only show your company that you're serious about your career, but you'll also meet some of the best people in your field," observed Keller of the ASTE. Among his other career tips, especially targeted to young engineers:

- Keep a daily log of your engineering activities, so managers can better understand your contributions,
- Take some business courses and investigate forming your own company,
- Understand what is happening on an international scale in your field, and
- Publish papers and attend conferences in your specialty as a way to build your network.

What are the three biggest challenges you face on the job?

Time pressures	73%
Increasing number of projects	53%
Keeping up with new technology	36%
Taking on additional engineering functions	36%
Unclear company/division strategies	31%
Reducing the cost of test/measurement	29%
Other	6%

The essential role of test

All these suggestions boil down to the need for engineers to be more broader based and more business savvy than ever before. They will also need to get used to the fast development cycle and quick changes that mark today's companies. And that includes being able to roll with the punches as projects get scrapped for more marketable ideas.

Even so, observers see the test field as more than holding its own in the engineering hierarchy. Dement of National Instruments likes the fact that her test work gives her a glimpse of a wide range of new technologies before they reach the marketplace. Durstenfeld of RAE Systems sees solid growth in automated test as companies try to ramp up volume and squeeze more costs out of their manufacturing processes.

Still others predict a growing demand for test services, both from equipment suppliers and independent engineering consultants. "The test field will continue to grow," said Lewis of Arrow International. "Not only is there the need to meet the scrutiny of government regulations, but companies themselves want a lot more evidence to prove that a product will meet all performance requirements throughout its lifecycle." T&MW

Which one area are you most concerned about?

Job security	35%
Keeping current on technology	18%
Management support	15%
Sufficient operating budget	12%
Outsourcing	11%
Company merger or acquisition	5%
Keeping current on regulations	1%
Other	3%

WHAT'S YOUR TAKE?

Want to have your say about the state of the engineering profession? Check out chief editor Rick Nelson's blog, "Taking the measure," in which he comments on a variety of engineering topics, including globalization and the state of the engineering profession. Join in the discussion!

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Precision Alignment Enables Rapid Attachment of Raptor Wings

Customer Challenge: Mate two large fuselage sections of a supersonic fighter jet – Lockheed Martin's F/A-22 Raptor – with an accuracy of 0.004 inches across 18 wing lugs on each side of the aircraft over a 16 foot wing root. Approximately half of the wing lugs are on the mid-fuselage section, while the other half are on the aft-fuselage.

DVT Solution: DVT certified integrator Delta Sigma Corporation, working with Automation Solution Provider Advanced Control Solutions, placed a DVT Smart camera inside of a "pin" that was the identical size of the pins that attach the wing to the fuselage. There are 16 of these special "vision pins" which are placed into jigs that simulate an ideal wing. While the cameras monitor the position of the key fuselage points and supply real-time 3-dimensional data to the control computer, the computer sends position commands to 14 servo motors that position both of the fuselage sections in six degrees of freedom with an accuracy better than 0.001 inch. When the alignment is complete – typically a 30 second operation – the fuselage sections have relative positions for ideal wing attachment.

For more information visit Delta Sigma Corporation at: **www.deltasigmacorp.com**; or Advanced Control Solutions at: **www.acs-ga.com**.

Roger C. Richardson
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Photo of F/A-22 Raptor courtesy Edwards Air Force Base.

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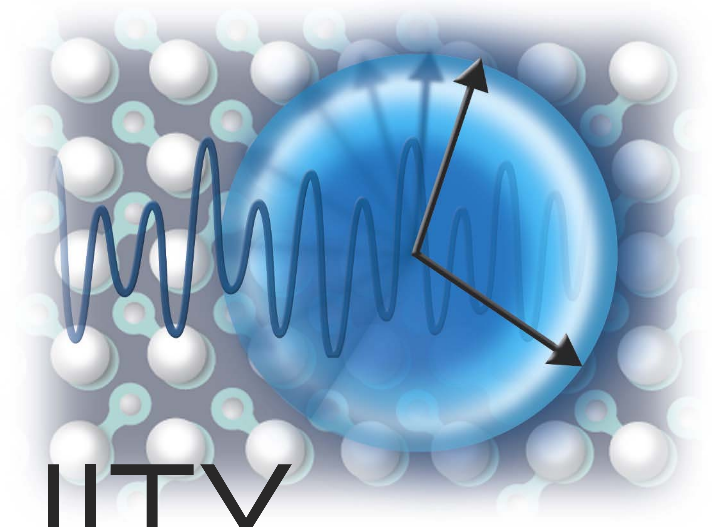

Array packages with high I/O counts require new test techniques for screening out wire-bond and other defects.

CONTINUITY TESTING

C.H. LIM, NATIONAL SEMICONDUCTOR

As semiconductor packages grow more complex, conventional continuity tests are no longer adequate for screening out open circuits and pin-to-pin shorts. Most test methods were designed for devices with pins aligned on the peripheral of the package. On today's micro surface-mount-device (SMD) and ball-grid-array (BGA) packages, however, the pins are aligned in a matrix—an arrangement that demands a new test approach.

In a typical continuity test, the test equipment applies a small current (usually a few milliamps) in parallel to all pins and measures diode turn-on voltage for each pin to verify continuity between the tester and the internal die. With the appropriate limit set for the expected diode-drop voltage for each pin, a single parallel continuity test can screen for parts with open I/Os.

Such a parallel continuity test can also detect shorted I/O pins, as long as the short causes the pin output voltage to swing away from a typical diode-drop voltage—for instance, to ground or to a high-voltage state. But a parallel test is ineffective at catching a short that produces an insignificant voltage difference.

To screen for such shorts, you can employ other parametric or functional tests, but by using such an indirect method, you risk losing the ability to indirectly screen some shorted pins when production test steps become consolidated as a device matures. In addition, indirect continuity testing might not detect a short between devices where adjacent I/O pins do not exhibit significant functional differences, such as two output channels of separate but similar voltage regulators.

Obviously, you need to use a different method to guarantee that all tested parts are free from potential shorts between pins. The solution needs to take into account the complexity of matrix, or two-dimensional, I/O arrangements, without significantly increasing the test time and cost.

The matrix arrangement of today's package types significantly increases the probability of two or more

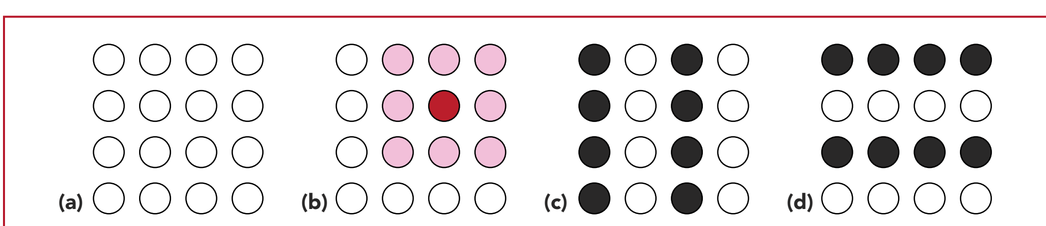

FIGURE 1. (a) A grid arrangement provides many possibilities for pin-to-pin shorts. (b) The red pin could be shorted to any of the eight pink pins. (c) Black I/O pins are grounded, while the white I/O pins are tested for continuity. A test setup can detect horizontal and diagonal shorts between I/O pins. (d) Reversing the black and white I/O setups enables detection of vertical shorts.

pins being shorted together, as a pin in the center of the package could be shorted to any of the pins surrounding it. But doing a continuity short test on two adjacent I/O pins for every combination would be counterproductive, especially as the I/O count increases.

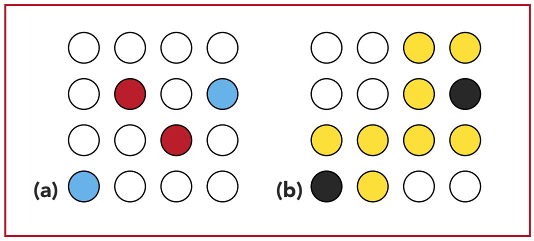

FIGURE 2. (a) This 16 I/O pin configuration has multiple supply (red) and ground (blue) I/O pins. (b) Ground potential (black) is established at the device ground I/O pins, and continuity is measured on all white (nonadjacent) and yellow (adjacent) pins.

The black & white continuity test

One method that shows promise for using ATE to detect opens and shorts without sacrificing test efficiency is a technique that I call the "black & white" continuity test. The black & white continuity test attempts to use a minimal set of test conditions to detect all potential shorts between two or more pins on a package.

In conventional pin-to-pin continuity test, the test iteration depends on the I/O count. For an I/O matrix of m x n where m is the number of rows and n is the number of columns, it takes (m x n) – 1 iterations to detect all potential shorts.

For typical ATE, the continuity test alone can take 1 s or more when the I/O count exceeds 100. The black & white test method, however, can hold continuity test time to tens of milliseconds, regardless of the number of I/O pins. The only additional test time required for this method involves tests needed for pins that cannot be toggled to ground.

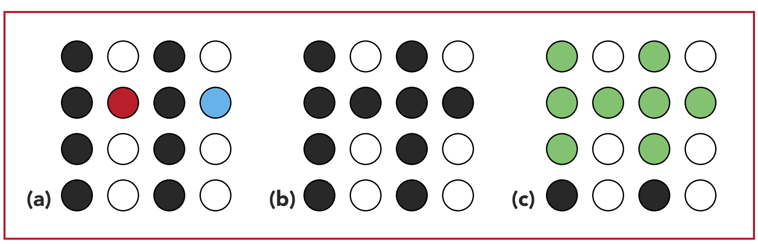

FIGURE 3. (a) Black pins are grounded while white I/O pins are tested for continuity. Red and blue pins are effectively grounded because of internal die connections and are shown in black in (b). The green pins in (c) represent undetectable shorts.

In the configuration shown in **Figure 1a**, a short between two adjacent pins can occur in many different ways. For each fully surrounded pin (such as the red pin in **Figure 1b**), there are at least eight possible ways for a short to occur.

A lengthy way to ensure that ATE can detect each possible short is to force a ground potential across all the pink I/O pins and test the red I/O for continuity. Should a short occur, the tester would measure a ground voltage instead of a diode turn-on voltage on the red pin. This process would have to be repeated for the rest of the I/O pins to fully cover all the possibilities—clearly not an efficient option for high-pin-count devices.

The black & white continuity test method—derived from a checkerboard pattern—is more efficient. To fully test every pin for opens or shorts to adjacent pins, the black & white test method requires only three continuity test iterations, regardless of the number of I/O pins available on the package. It is applicable to all matrix-type packages, including micro SMD and BGA, and is even applicable to multi-row and multi-column in-line packages like high-pin-count leadless lead-frame packages (LLP).

The first continuity test iteration tests for opens on all of the pins in parallel. If any pin has an open circuit, it fails this test. In the second setup iteration (**Figure 1c**), the ATE drives black pins to ground to test the white pins. This test detects shorts occurring between diagonally or horizontally adjacent pins, but it will not detect shorts between vertically adjacent pins. The third iteration (**Figure 1d**) handles that final case.

Although the black & white test method attempts to reduce the number of iterations to three, situations inevitably arise that demand more iterations for complete coverage. One such situation arises because of supply and ground I/O pins. Another is mainly caused by the way the test hardware accesses the DUT (see "Test hardware design," p. 42).

Multiple supplies and grounds

For supply pins, it's common to use a supply-current test to guarantee continuity. Grounds, on the other hand, are commonly used as the reference for continuity testing. Some designs discourage forcing grounds to a potential higher than other I/O pins, as this could reverse-bias some circuits and damage the die. Therefore, testing supply pins and grounds for opens and shorts requires some planning.

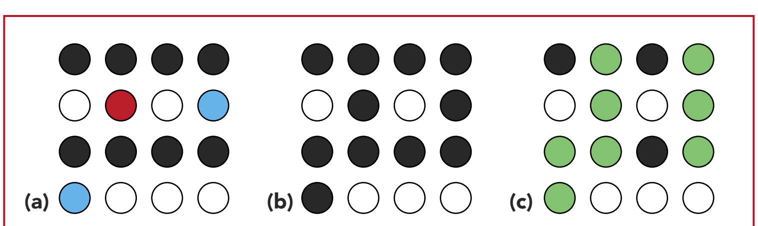

FIGURE 4. (a) The horizontal ground configuration can detect vertical shorts. (b) This figure shows the effective configuration with commonly connected device supply and ground I/O pins. (c) Pins shown in green are undetectable for shorts in the vertical direction.

Consider the I/O configuration shown in **Figure 2a**, where the red I/O pins are supplies and the blue I/O pins are grounds. To test for continuity, you must first identify which I/O pins are supplies and grounds and then apply the black & white steps. First, test for opens on all pins in parallel. Then, force ground

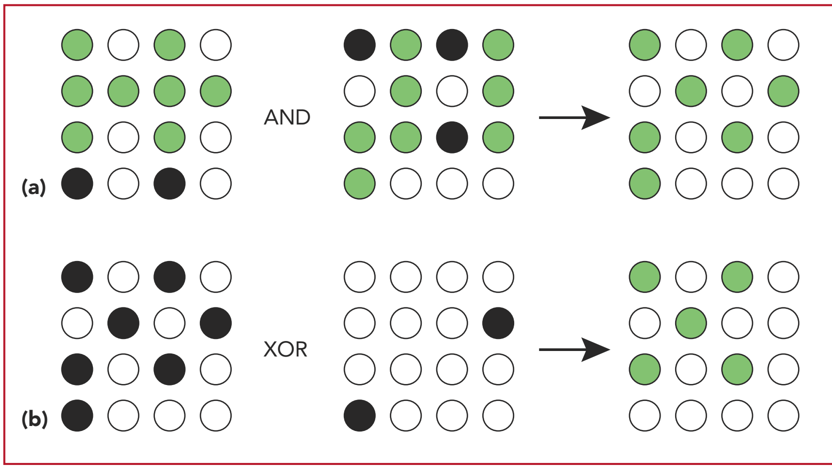

FIGURE 5. (a) A logic AND function can determine I/O pins with at least one undetectable short to an adjacent I/O pin. (b) An XOR logical function determines the final set of pins with at least one undetectable short possibility to an adjacent pin.

pins to ground potential. Note that any short between ground pins and their adjacent pins (yellow) would cause the continuity test to fail (**Figure 2b**).

Next, establish ground potential on alternate columns and measure continuity on remaining pins (**Figure 3a**). As the device supplies and grounds are usually connected together on the die, the effective configuration would appear as shown in **Figure 3b**. This second iteration can detect all horizontal and diagonal shorts on all white I/O pins. For a few combinations, however, detections are not possible. Horizontally and diagonally adjacent pins that cannot be detected for shorts are shown in green in **Figure 3c.**

The next iteration detects vertical shorts by switching the vertical black (grounded) I/O pins to horizontal (**Figure 4a**). For continuity testing, at least one device ground is set to ground potential. Again, because supplies and grounds on the die are commonly connected, the resultant configuration is as shown in **Figure 4b**. To check for non-testable pins,

Test hardware design

For devices sensitive to noise, test engineers often place emphasis on ensuring that a board is designed for optimum functional and parametric performance, and they don't pay much attention to continuity testability. As a result, such boards might not have the flexibility to allow a thorough pin-to-pin test for both opens and shorts.

For efficient use of the black & white test method, you should have test hardware that can directly access every pin under test except for supply and ground pins. In the best scenario, you'll use relays to provide onboard isolation of supplies and grounds so that despite a die-level short on these I/O pins, you can still test for opens on individual pins.

In many situations, a test engineer needs to choose between having the ability to individually test every pin for opens and for adjacent shorts and having the ability to test for other performance characteristics that might override the risk associated with not being able to detect continuity failures up front. Some of the considerations might include:

- supply and ground noise,
- impedance mismatch,
- trace capacitance or inductance, and
- tester resource availability.

A lot of functional and parametric tests can indirectly screen out continuity defects. An assessment is usually required to determine the coverage at the end of the day.—*C.H. Lim*

scan vertically for pins under test that do not fall next to a black pin in the same column. These non-testable pins are highlighted in green in **Figure 4c**.

Performing an AND operation (**Figure 5a**) on all green I/O pins in Figures 3c and 4c can check for any pin that cannot be tested for a short. All black and green pins are treated as logic 1, while all white pins are treated as logic 0. (Note that if two corresponding pins are black, the results of the AND operation can be ignored since both of these I/O pins could be detected for shorts in the first place. These I/O pins are redundant in this analysis.)

Finally, apply an exclusive-OR (XOR) operation between the output from the logic AND operation (**Figure 5b**) and the parallel continuity test configuration from Figure 2b. The final iteration to test for pin-to-pin shorts is now to set the device supplies and grounds to ground potential and then test for continuity on the remaining pins with undetectable shorts (**Figure 6**).

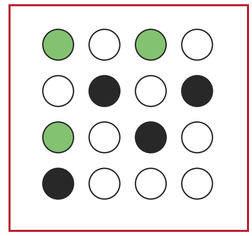

FIGURE 6. The final step is to ground all supply and ground pins and test for continuity on green I/O pins.

Here, a four-iteration continuity test is sufficient to detect all possible shorts between two adjacent pins compared to 15 iterations for a thorough per-pin continuity check. You can download a table that summarizes these steps at the online version of this article at www.tmworld.com/archives. T&MW

C.H. Lim *is a senior section test engineering manager for National Semiconductor in Melaka, Malaysia. He oversees IC testing for a variety of products, and he is involved in developing test manufacturing processes to support new products. Lim received his bachelor's degree in electrical and electronic engineering from the University of Leicester, UK.*


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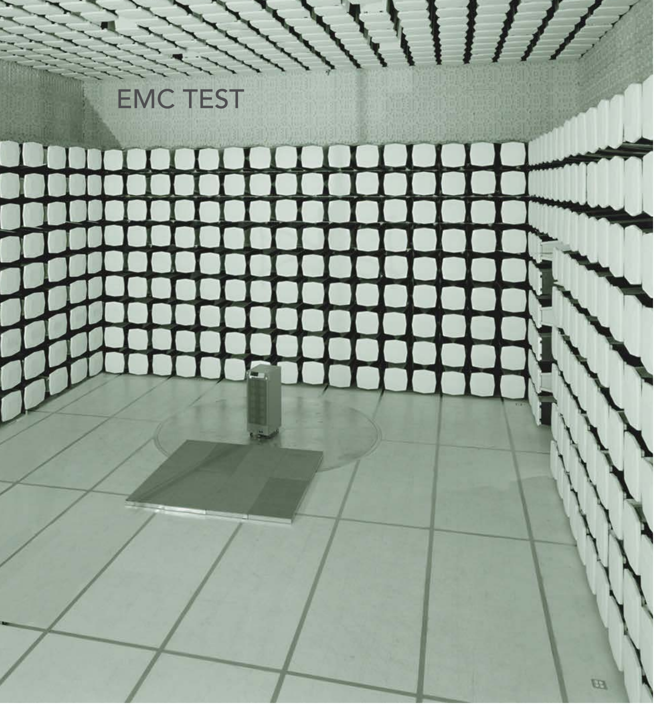

QUICK EMC SCREENING

SIMPLE COMPONENT TESTS MINIMIZE THE RISK OF NONCOMPLIANCE AND CUT EVALUATION TIME BY 70%.

MICHAEL TAYLOR, HACH CO.

Market pressures push manufacturers to cut manufacturing costs, which forces engineers to look for low-cost active and passive alternative components to use in mature products. Unfortunately, replacing a component may come with a price—it may force a product out of EMC compliance.

A component change typically necessitates two to five days of EMC emissions and immunity testing. When our compliance group became overwhelmed with the volume of component change requests, we knew that we needed a new testing approach. We now evaluate a component's characteristics and its function in the circuit before installing it into a product. The result: We cut component evaluation time by more than 70%.

In our method, we separate active and passive components and then use a two-tiered approach to evaluate the components for their effects on EMC compliance. At tier 1, we review a component's parametric values and its function in a circuit. From this analysis, we can show that certain electrical parameters have a significant effect on compliance, while others have little or no effect.

Figure 1 shows our evaluation process. If we determine that a part needs evaluation, we test it on an Agilent Technologies 4395A network analyzer. We measure impedance magnitude (|Z|), capacitance (C), phase (θ), dissipation factor (D), inductance (L), and quality factor (Q) as functions of frequency.

From a |Z| measurement, we can find a component's resonant frequency. If a low-cost replacement component such as a capacitor has a lower resonant frequency than an existing component, it won't suppress noise well enough for our product to meet compliance specifications, and we

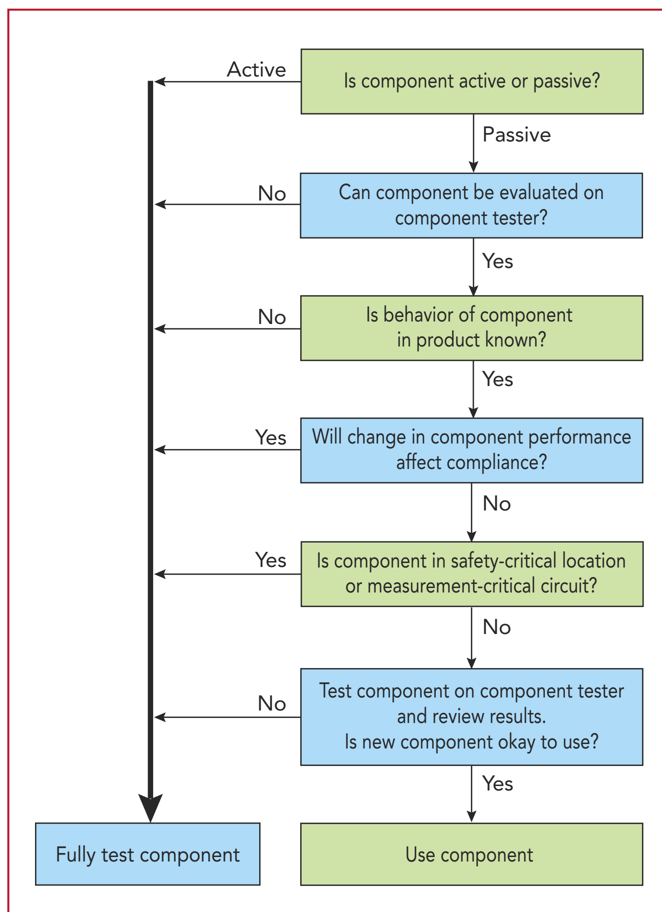

FIGURE 1. Using this evaluation procedure, we determine whether a component meets all review criteria for replacing an existing component.

PHOTO: ETS-LINDGREN

reject it. If the component's performance parameters are equal to or better than the original component in its intended function, then we conclude that the risk of using the new component is acceptably low.

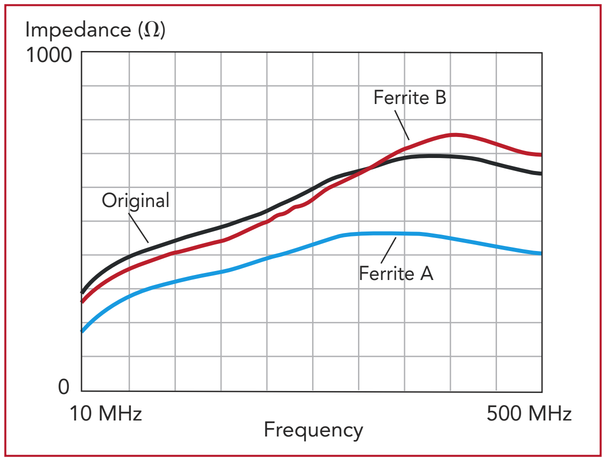

FIGURE 2. Low-cost ferrite A (blue) failed to perform as well as an existing component, but ferrite B (red) performed better than the original at high frequencies.

Measured results

To illustrate our method, we used our tier-1 process to evaluate two possible replacements for a ferrite. When correctly applied in a circuit, ferrites can reduce emissions—the critical parameter is impedance versus frequency. **Figure 2** shows the impedance of the two low-cost replacements compared to that of the original one. The plot shows that low-cost ferrite A (blue trace) produces an impedance below the minimum required by this circuit. Ferrite B (red trace) from another supplier, however, has an impedance somewhat greater than the existing component at high frequencies for noise suppression. Ferrite B will meet the requirements for the circuit in question. Ferrite A won't.

Using the tier-1 process, we reduced the evaluation time from hours to minutes. Our old method of a full compliance test required us to bring a finished product to our anechoic chamber for emissions testing. It required at least an hour to build a circuit board, install it in a product, verify operation, and deliver the product to the compliance engineering group. We then needed at least another hour to perform a radiated-emissions test.

Compare that to the 10 min we need to perform the parametric measurement with the component analyzer. We save 1 hr, 50 min. Multiply this over 10 components per week, and the labor savings exceed one person-day each week. Our new method has proven invaluable in rapidly separating the acceptable replacement components from components that will likely cause problems.

Modified immunity test

In cases where a component evaluation is insufficient to tell us whether a low-cost component will create compliance issues, we turn to tier-2, a modification of our diagnostic immunity testing procedure. Tier-2 testing isn't a replacement for full compliance certification, but it quickly identifies susceptibility issues that result from a component substitution.

The tier-2 procedure compares test results from a modified product to an existing product. To make the comparison, we need an immunity model of the existing product, which we developed during the product's full compliance certification testing. We store each model's compliance test data in a technical information file, a derivative of the technical construction file formerly used for EU competent-body certification.

The tier-2 method modifies some of the immunity tests to minimize testing time. We currently use the tier-2 method for radiated immunity, conducted immunity, electrical fast transient, and surge tests.

We base our modified radiated and conducted immunity tests on a circuit's ability to respond to impinging RF energy. The response may be difficult to identify because of software averaging, but given repeated exposure, the response will become detectable. EMC standards EN 61000-4-3 (radiated immunity) and EN 61000-4-6 (conducted immunity) for CE compliance require that a product be exposed to RF energy for at least one complete product-operation cycle for each frequency step, called the dwell time.

Unfortunately, dwell time can take up to 20 min for some of our products because of long operational cycles. To complete a cycle, some analytical instruments must wait for a chemical reaction in a sample to take place, which can take up to 20 min. We can, however, reduce the product's dwell time for compliance testing by using pre-reacted samples and special test firmware in the instrument under test. Even so, some products can still take as long as 15 min to complete an operation cycle.

(continued)

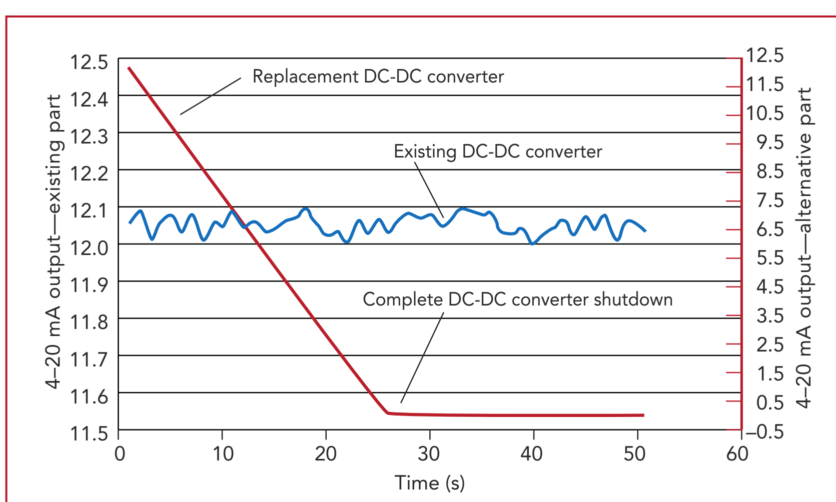

FIGURE 3. A replacement DC-DC converter failed a swept-frequency immunity test. Unlike the original part, the replacement part shut down during a test.

Even if a product's cycle time is short, say 20 s, a radiated immunity test can still take hours because we must subject the product to RF energy at many frequencies. The current radiated immunity test standard requires testing from 80 MHz to 1000 MHz at 1% frequency steps on all four sides of the equipment under test (EUT) at both horizontal and vertical polarities. If we add all the frequency steps, sides, and polarities, we must complete 2040 steps (255 frequencies x 4 sides x 2 polarities). If each step takes 20 s, then 2040 steps will take 40,800 s, or 11.3 hrs of test time.

For conducted immunity tests, the frequency test range is 0.150 MHz to 80 MHz in 1% frequency steps, or 633 frequency steps. At 20 s/step, that adds up to 12,660 s, or 3.5 hrs. Thus, we need 14.8 hrs—nearly two full work days—to complete both the radiated and conducted immunity tests for a full compliance test.

Our tier-2 process shortens this time considerably. Instead of waiting for the product to complete an operational cycle for each frequency step, we sweep through the *entire* frequency range in 5 s to 20 s. We make up to 100 frequency sweeps for each operation cycle of the EUT.

Obviously, this method would not be acceptable for full compliance testing, but it is fine for evaluating a product's immunity. If we don't detect a response from the sweeps, then we conclude that switching to a low-cost component won't cause the product to fail a full compliance test. If we do detect a response, then we subject the product to full compliance testing to determine the exact response frequency.

To understand the time savings, assume a mean of 50 frequency sweeps at 5 s per sweep. We would thus need 250 s (4.16 min) to test each of a product's four sides at both horizontal and vertical polarities—a total of 33.3 min per product.

For the conducted immunity test, we need just one frequency sweep test at 4.16 min. Thus, we need a total of 37.5 min (0.62 hr) to perform both radiated and conducted immunity tests—a savings of 14.18 hrs (1.78 work days) over the 14.8 hrs needed for a full compliance test.

To perform a frequency sweep, we use an RF signal generator to drive a power amplifier and an antenna. We measure the field strength with an isotropic field probe. The probe's controller has an analog output that we feed into the amplifier's automatic gain control input.

Further time savings

We can achieve similar time savings for electrical fast-transient and surge testing by subjecting the product to the most severe interference levels only. With our products, we have data to indicate that if the product passes under the most stressful conditions, it will pass under lower stress levels. If we detect a failure, we can analyze it by performing a full immunity test. At this level of evaluation, we're looking for a simple yes/no result. That is, does the product containing the low-cost component respond differently from the original instrument?

Figure 3 shows the results of a swept test of an existing and a proposed alternate DC-DC converter. We use the converter to power an instrument controller's isolated 4–20-mA output. The original component showed no meaningful response when subjected to a sweep. The proposed replacement however, not only lost regulation, it shut down halfway through the test. The converter regained regulation after testing. Clearly, the substitute component is not a suitable replacement.

If you want to try a method similar to the one we use, you first need a compliance history of your product. That is, make sure you have a full emissions and susceptibility profile to compare the test results against. Without a known set of behavior, you can overlook a minor response. With a known product profile, you can carefully watch for minor anomalies during rapid testing. If in doubt, perform a full compliance test. T&MW

Michael Taylor, *NCE, is principal EMC compliance engineer at Hach Co., the Environmental Water Quality Division of Danaher Corp., based in Loveland, CO. He has degrees in mathematics and electrical engineering and has worked in the EMC field for more than 30 years.*

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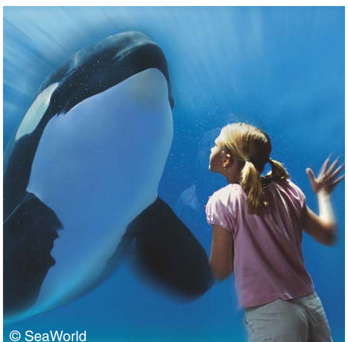
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Excite and analyze serial buses

Serial buses such as PCI Express and SerialATA are pushing bit rates beyond 3 GHz, making their signals look like microwaves traveling through copper traces. To test such high-speed signals, Agilent Technologies has introduced a 7-GHz pulse generator and added S-parameter analysis to its DCA-J sampling scopes.

The 81141A ($88,000, pictured) lets you produce PRBS serial data streams, clock signals, pulses, and real-world data to test receivers and data channels. It produces PRBS streams at up to 2^{31}–1 bits, and it lets you adjust duty cycles in clock signals. You can add jitter by connecting a function generator to the 81141A; the unit will modulate the signal onto its output pulses. The 81141A lets you select from return-to-zero (RZ), non-return-to-zero (NRZ), and return-to-one (R1) data patterns.

To test transmitters and data channels, Agilent has added an S-parameter option ($6000) to its DCA-J line of sampling scopes. The option, which you can download and install, lets you analyze pulsed signals in the frequency domain. *Agilent Technologies, www.agilent.com.*

Code Composer Studio gains rewind feature

Texas Instruments has announced the release of the Platinum Edition of its Code Composer Studio integrated development environment (IDE). The Platinum Edition makes code debugging less frustrating by introducing two new features that can save developers significant time when tracking down pervasive bugs: The CCStudio Rewind feature allows programmers to back-step through their source code with a single keystroke, while the new Connect/Disconnect feature enables developers to "hot swap" a target board in seconds to eliminate hardware suspects during debug.

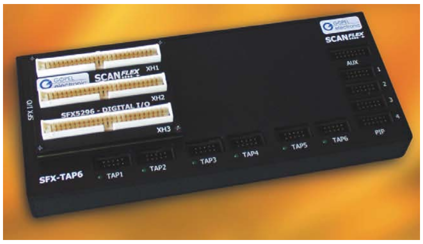
To address the many DSP applications that are growing to hundreds of thousands of lines of code with onboard support for multiple processors, CCStudio Platinum Edition is a fully merged IDE supporting all TI platforms, including the TMS320C6000 DSP, TMS320C5000 DSP, TMS320C2000 DSP, and OMAP platforms. Other features include a component manager that lets users upgrade their IDE to take advantage of new features and bug fixes while locking down on a specific compiler and DSP/BIOS software kernel foundation version. The new component manager also lets the developer install and evaluate a new compiler or DSP/BIOS kernel version before committing to it.

Price: $3600, including 15 months of update subscription service. A free 120-day evaluation version is available on CD-ROM. *Texas Instruments, www.ti.com/ccstudioplatinumpr.*

Scanflex boundary-scan products debut

Goepel electronic has announced the availability of several products for extended boundary-scan implementations based on its new Scanflex architecture. This wave of Scanflex products includes the SFX/PCI1149 PCI-based Scanflex boundary-scan controllers, which operate at 20, 50, or 80 MHz; Scanflex TAP transceivers, which come in 2-, 4-, 6-, and 8-TAP standard configurations as well as 2- and 4-TAP compact versions for rugged environments; and the SFX5296 Scanflex I/O module, which provides 96 parallel I/O channels.

The SFX controllers are upgradeable on the fly while residing within a host PC. They include compensation for signal propagation delay and support dynamic data synchronization of serial and parallel vectors. The TAP transceivers include resources such as 32 dynamic, parallel digital I/O channels, two analog I/O channels, three static digital I/O channels, and trigger lines. Furthermore, they feature removable TAP Interface Cards (TICs). The first available TIC—a single-ended interface with line drivers supporting TAP cable up to 1.5 m long—provides programmability for input threshold, output voltage, input and output impedance, TCK frequency, delay compensation, a relay-controlled power signal, and read-back capability of TAP output signals.



For the I/O module, each of the 96 I/O channels is individually configurable as input, output, bidirectional, or high impedance. Users can program I/O voltages in groups of 32 channels. The SFX controller, I/O modules, TAP transceiver, and TIC can be combined in any configuration with distances between controller and TAP transceiver extending to 5 m. Scanflex works with the company's System Cascon boundary-scan software environment (version 4.2.1 and up).

Starting price: $3500. *Goepel electronic, www.goepel.com.*

> > > > > > >

TDR hand probes

Able to accommodate a wide range of differential line spacings on PCBs, the P80318 and P80318X 18-GHz TDR hand probes greatly improve differential TDR measurement integrity for electrical serial data signals. Each probe can resolve small spatial features used to determine the differential impedance and if differential lines are matched in length. Probe pitch is continuously adjustable from 0.5 mm to 4.2 mm (signal to signal). The P8018 and P80318X are functionally identical, but the P80318X comes with a second probe body. Base price: $3990. *Tektronix*, www.tek.com.

T1/E1 analyzer software

The T1/E1 Analysis Suite provides comprehensive analysis and emulation capabilities for voiceband and signaling protocol analysis. New and enhanced applications in Version 4.86 include delay attenuate timeslots with very low echo path delays (for HD boards only), TRAU traffic playback, PPP protocol analysis, UMTS protocol analysis, remote voiceband activity detector, and instant client analysis. *GL Communications*, www.gl.com.

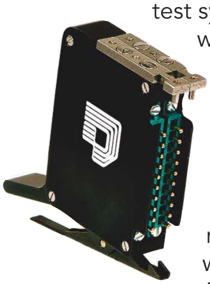
Isolated data acquisition

Members of the DI-718B series of data-acquisition instruments employ integrated isolated amplifiers that record data to removable Secure Digital (SD) memory cards. Depending on the model, the 14-bit, eight-channel instruments either stream data to a PC or collect data as a stand-alone datalogger. Each type is available with either a USB or Ethernet interface. All DI-718B products have eight analog input channels, each of which is capable of accepting a DI-8B amplifier module. Price range: $595 to $895. *DATAQ Instruments*, www.dataq.com.

Development tool

National Instruments' LabView Embedded Development Module extends LabView to any 32-bit embedded processor, providing a graphical approach to algorithm design, simulation, prototyping, and deployment of custom designs for embedded systems.The module includes more than 400 analysis functions for signal processing, linear algebra, curve fitting, statistics, and calculus. What's more, it features a framework for integrating I/O drivers and board support packages for taking advantage of specific processors with LabView. *National Instruments*, www.ni.com.

Cable test equipment adapter



Manufactured in groups of 10 pins, the EasyMate interface connector adapts DIT-MCO cable and harness test systems to reduce wasted nodes and minimize adapter cable complexity. The connector's low contact resistance enables a high number of cycles without degradation. It also offers low current-carrying capability, smooth wiping action during engagement, and all-metal construction to resist damage due to forceful handling and repetitive movements. *DIT-MCO International, www.ditmco.com.*

180-W power supply

Delivering 9.6 W/in.^{3} in a 3x5-in. footprint, the NV-180 single-output AC/DC power supply achieves up to 90% efficiency for use in high-density medical, process control, and test and measurement equipment. It is initially available with outputs of 5 V, 12 V, and 24 V and with currents of up to 25 A. The unit also offers an optional high-power standby output rated at 5 V/2 A, remote on/off, and power good signal. The NV-180 carries EN60601 medical approval combined with EN55022 Level B conducted emissions, as well as EN61010 and EN60950 approvals. Price: $89 (100 units). *Lambda, www.lambdapower.com.*

Wireless strain-gage system

The Model i400 wireless telemetry and strain-gage sensor system comprises two 915-MHz digital telemetry modules. The sensor end module includes an embedded SensorData i200 AC strain-gage conditioner and a 16-bit sigma-delta ADC. The receiver end module couples through its onboard RS-232 port to the serial port of a PC or PLC. A switch-selectable analog output signal of ±5 VDC or ±10 VDC is standard on the receiver module. The i400 is compatible with any SensorData rotating torque sensor, non-rotating torque sensor, or any device supplied by SensorData with a strain-gage bridge sensing element. PC-compatible software is included. *SensorData Technologies,* www.sensordata.com.

IC test system

Boasting a compact 11x14-in. footprint, the IC-100 general-purpose IC test system is small enough to sit on top of most handlers and probers, yet powerful enough to allow for high-throughput end-of-line testing. The system offers a choice of three different standard test heads for testing analog and discrete ICs up to 128 pins. Test program development is done using an intuitive fill-in-the-blanks spreadsheet that can be written and compiled offline. Its streamlined software also minimizes test costs and reduces test times. Most internal calculations are precompiled before actually testing the device, and many setups and housekeeping tasks are performed during the prober/handler cycle time. Base price: $30,000. Delivery: 6 to 8 weeks. *Production-Line Testers,* www.production-linetesters.com.

CompactPCI/PXI DAC

Built on a single-width, 6U CompactPCI/PXI module, the CP266 digital-to-analog converter card supplies 64 analog-output channels with 16-bit resolution and ±10-V full-scale output range. You can set the power-up state of the analog outputs to independent user-defined values to provide non-zero voltage

▷ Visit **www.tmworld.com/webproducts** for Web exclusive product writeups settings on application of power. The channel update rate is 2 ms, and each output is accurate to within ±1 mV. Paired output signals eliminate ground offset effects. Typical applications include automotive test cells, industrial control, and automated test equipment. Price: $2750. Delivery: 4 to 6 weeks. *KineticSystems, www.kscorp.com.*

High-speed vision sensor

Combining fast sensing speed with high resolution, the PresencePLUS P4 Edge 1.3-Mpixel vision sensor performs up to 1200 inspections/min at a cost of under $2000. The P4 Edge uses a 1280x1024-pixel imager to

capture minute details of multiple features at ranges from a few inches to several feet, depending on the lens. You can use the compact, self-contained vision sensor for precision inspections, error-proofing, and counting stamped metal parts, as well as for validating the location of objects such as labels or components of an assembly. The P4 Edge offers a built-in Ethernet connection, RS-232 port, or four discrete input/outputs, along with either an in-line or right-angle lens. Price: $1995. *Banner Engineering, www.bannerengineering.com.*

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ROBERT HUM
VP & General Manager
Design Verification and Test Division
Mentor Graphics
San Jose, CA

Robert Hum joined Mentor Graphics with Mentor's acquisition of IKOS Systems in 2002. Hum has more than 25 years of experience in engineering, marketing, business development, and operations. Most recently, he served as the executive VP and COO of IKOS, and he has also held senior business and technology management positions at Cadence Design Systems and Bell-Northern Research (Nortel). Hum has an MSEE from McGill University in Montreal, QC, Canada.

DFT drives yield improvement

At Mentor Graphics, Robert Hum is responsible for verification tools such as 0-In, ModelSim, and Questa, and for DFT tools such as TestKompress. Chief editor Rick Nelson spoke with him at the Design Automation Conference and followed up with a phone interview.

T&MW: At DAC, you said that more than 50% of design is verify and test. Could you explain?

Hum: Several studies have measured how many engineering hours go into certain activities. About a third of the design activity involves translating written specs in English into RTL. The other two thirds of the time is verification. It's writing functional test benches and verifying that your design, in fact, does meets the spec and that you have correctly implemented it.

T&MW: What verification and test products does Mentor offer?

Hum: On the design-verification side, we offer ModelSim and Questa. For test, we offer FastScan ATPG and TestKompress as well as built-in self-test products for both logic and memory. We also offer a boundary-scan product called BSDArchitect.

T&MW: TestKompress was introduced in part to address vector-memory limitations on test hardware—are memory limitations still a problem?

Hum: Yes. The memory problem on testers has gotten much worse. The number of vectors generated these days is absolutely enormous. There are two things to worry about: One is the amount of memory you have on a tester, and the other is test time.

While memory is pretty cheap these days, the problem with putting more memory on testers is that you then have to clock all the test vectors into your part, and on scan chains you generally limit the clock speed because of power problems, increasing test times drastically. So, TestKompress's ability to compress test vectors and reduce test time is very important.

T&MW: What is driving interest in design for yield (DFY)?

Hum: Yield learning is taking a lot longer than it did. Folks typically use test chips to determine basic transistor characteristics and to calibrate Spice models. Library vendors then build models that run on simulators and timing analyzers, and people construct various geometries to calibrate their OPC [optical proximity correction] processes and, when that's done, say this node is now ready for production. But they do their first couple of masks and get their first chips through and find yield isn't what they expected. They scratch their heads and ask what happened. DFY can prevent these kinds of problems.

T&MW: What is the next level in DFT?

Hum: The next level is going to be its application to this yield enhancement. If you have made an investment in scan design, you will be able to use your investment to analyze, control, and improve yield. We believe the next level of DFT is going to be the addition of diagnostics so you'll be able to diagnose thousands of parts rather than tens of parts per design, as you do today.

T&MW: Have test-bench languages like e and Vera had a positive effect on errors?

Hum: With any new technology, you need to ask what value it adds. A technology can make you more productive while not fundamentally changing what you are doing, or it can represent a shift in methodology that improves productivity and solves a problem. My research shows that the use of test-bench languages such as Vera and e has had a productivity impact but no discernible impact on the number of errors per design. If you had two spins per design before buying into Vera or e, you will still have two spins per design afterward. T&MW

▸ *The online version of this interview includes more Q&A with Robert Hum, where he describes in detail Mentor's verification and test offerings and elaborates on the future of DFT:*

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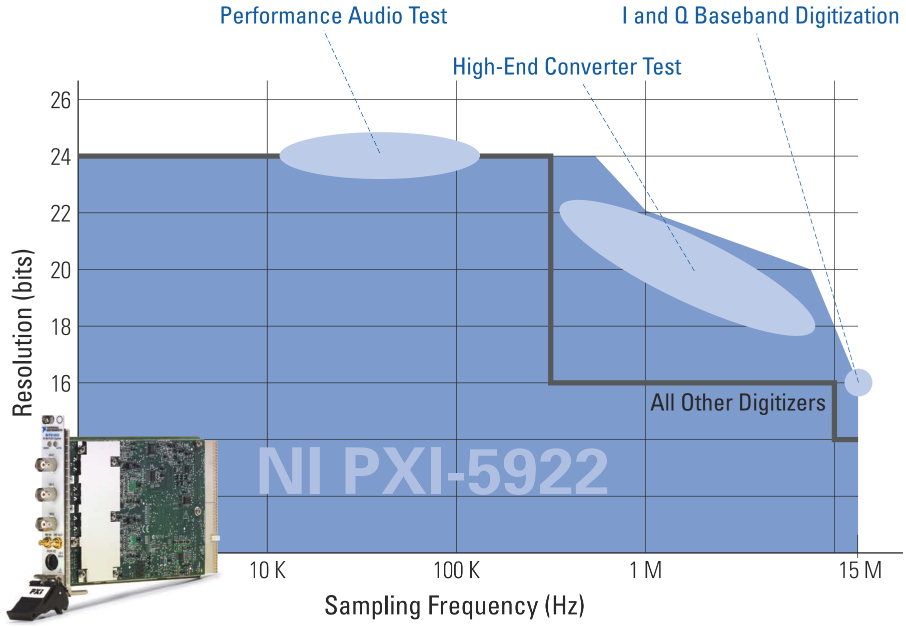

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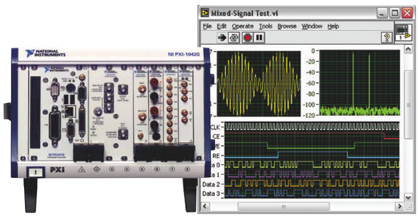

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